DAQ

NI 6052E User Manual

Multifunction I/O Device for PCI/PXI/1394 Bus Computers

November 2001 Edition
Part Number 370477A-01

Worldwide Technical Support and Product Information

ni.com

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FCC/Canada Radio Frequency Interference Compliance*

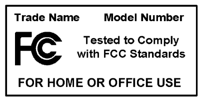
Determining FCC Class

The Federal Communications Commission (FCC) has rules to protect wireless communications from interference. The FCC places digital electronics into two classes. These classes are known as Class A (for use in industrial-commercial locations only) or Class B (for use in residential or commercial locations). Depending on where it is operated, this product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.)

Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products. By examining the product you purchased, you can determine the FCC Class and therefore which of the two FCC/DOC Warnings apply in the following sections. (Some products may not be labeled at all for FCC; if so, the reader should then assume these are Class A devices.)

FCC Class A products only display a simple warning statement of one paragraph in length regarding interference and undesired operation. Most of our products are FCC Class A. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

FCC Class B products display either a FCC ID code, starting with the letters **EXN**, or the FCC Class B compliance mark that appears as shown here on the right.



Consult the FCC Web site at `http://www.fcc.gov` for more information.

FCC/DOC Warnings

This equipment generates and uses radio frequency energy and, if not installed and used in strict accordance with the instructions in this manual and the CE Mark Declaration of Conformity**, may cause interference to radio and television reception. Classification requirements are the same for the Federal Communications Commission (FCC) and the Canadian Department of Communications (DOC).

Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.

Class A

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Class B

Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Canadian Department of Communications

This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe B respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

Compliance to EU Directives

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To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.

* Certain exemptions may apply in the USA, see FCC Rules §15.103 **Exempted devices**, and §15.105(c). Also available in sections of CFR 47.

** The CE Mark Declaration of Conformity will contain important supplementary information and instructions for the user or installer.

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About This Manual

This manual describes the electrical and mechanical aspects of the National Instruments (NI) PCI/PXI-6052E and the NI DAQPad-6052E for 1394 and contains information about operation and programming.

The NI 6052E is a high-performance multifunction analog, digital, and timing I/O device for PCI, PXI, or 1394 computers. Supported functions include analog input (AI), analog output (AO), digital I/O (DIO), and timing I/O (TIO).

Conventions Used in This Manual

The following conventions are used in this manual:

<>	Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DBIO<3..0>.
♦	The ♦ symbol indicates that the following text applies only to a specific product, a specific operating system, or a specific software version.
	This icon denotes a note, which alerts you to important information.
	This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.
1394	1394 refers to a high-speed external bus that implements the IEEE 1394 serial bus protocol.
bold	Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options. Bold text also denotes parameter names.
CompactPCI	CompactPCI refers to the core specification defined by the PCI Industrial Computer Manufacturers Group (PICMG).
italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.
`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples.

	This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.
NI PCI/PXI-6052E	Refers to the NI PCI-6052E and the NI PXI-6052E.
platform	Text in this font denotes a specific platform and indicates that the text following it applies only to that platform.

Related Documentation

The following documents contain useful information related to this product:

- *CompactPCI Specification, PICMG 2.0 R3.0*
- *DAQ-STC Technical Reference Manual*
- NI Developer Zone tutorial, *Field Wiring and Noise Considerations for Analog Signals*, located at `ni.com/zone`
- *PCI Local Bus Specification,* Revision 2.2
- *PXI Specification,* Revision 2.0

1 Introduction

This chapter describes the NI 6052E, lists what you need to get started, describes optional software and optional equipment, and explains how to unpack the device.

About the NI 6052E

Thank you for buying an NI 6052E. The device has the following features:

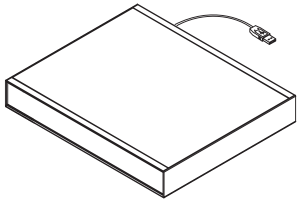
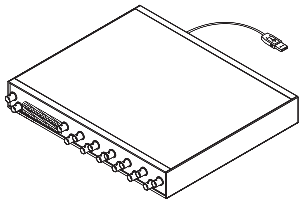
- Two 16-bit A/D converters (ADCs) with 16 analog inputs
- 16-bit D/A converters (DACs) with voltage outputs
- Eight lines of transistor-transistor logic (TTL)-compatible DIO
- Two 24-bit counter/timers for timing I/O

The NI PCI/PXI-6052E is a switchless, jumperless data acquisition (DAQ) device. This feature is made possible by the NI MXI Interface to Everything (MITE), which is a bus interface chip that connects the device to the PCI or PXI I/O bus. The MITE implements the PCI Local Bus Specification so that all the interrupts and base memory addresses are software configured. Because the device has no DIP switches, jumpers, or potentiometers, you can easily software configure and calibrate the device.

The NI DAQPad-6052E for 1394 is a high-performance, switchless, jumperless, hot-pluggable DAQ device. 1394 automatically handles the assignment of all host resources and allows you to install the device without turning the computer off. You can plug up to 64 National Instruments DAQ devices into a single computer using 1394, although you will run out of bus bandwidth if all devices operate at full rate. In addition, the NI DAQPad-6052E for 1394 provides up to 250 V of DC functional isolation from the computer.

There are two versions of the NI DAQPad-6052E. Table 1-1 illustrates the different I/O connectivity and form factors of each version.

Table 1-1. NI DAQPad-6052E Models

Model	I/O Connector
DAQPad-6052E 	68-pin SCSI II Male
DAQPad-6052E for BNC 	BNC and removable screw terminals

The NI 6052E uses the National Instruments DAQ-system timing controller (DAQ-STC) for time-related functions. The DAQ-STC consists of three timing groups that control AI, AO, and general-purpose counter/timer functions. These groups have a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns. The DAQ-STC makes possible applications such as buffered pulse generation, equivalent time sampling, and seamless sampling rate change.

The NI 6052E uses the Real-Time System Integration (RTSI) bus to synchronize multiple measurement functions to a common trigger or timing event. The RTSI bus consists of the NI RTSI bus interface and a cable, and it routes timing and trigger signals between several functions on as many as five DAQ devices in the computer.

SCXI is the NI instrumentation front end for plug-in DAQ devices. The NI 6052E interfaces to an SCXI system so that you can acquire over 3,000 analog signals from thermocouples, resistance temperature detectors (RTDs), strain gauges, voltage sources, and current sources. You can also acquire or generate digital signals for communication and control.

Refer to Appendix A, *Specifications*, for specifications of the NI 6052E.

Using PXI with CompactPCI

Using PXI-compatible products with standard CompactPCI products is an important feature provided by *PXI Specification,* Revision 2.0. If you use a PXI-compatible plug-in card in a standard CompactPCI chassis, you cannot use PXI-specific functions, but you can still use the basic plug-in card functions. For example, the RTSI bus on the NI PXI-6052E is available in a PXI chassis but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI because the standard implementation for CompactPCI does not include these sub-buses. The NI PXI-6052E works in any standard CompactPCI chassis adhering to *CompactPCI Specifications, PICMG 2.0 R3.0.*

What You Need to Get Started

To install and use the NI 6052E, you need the following items:

- ❑ One of the following devices:
  - NI PCI-6052E
  - NI PXI-6052E
  - NI DAQPad-6052E for 1394
- ❑ *NI 6052E User Manual*
- ❑ One of the following software packages and documentation:
  - LabVIEW **(for PC compatibles and Mac OS[1])**
  - Measurement Studio **(for Windows)**
- ❑ NI-DAQ **(for PC compatibles and Mac OS[2])**
- ❑ The computer

[1] The DAQPad-6052E for 1394 does *not* support LabVIEW for Mac OS.

[2] The DAQPad-6052E for 1394 does *not* support NI-DAQ for Mac OS.

Software Programming Choices

When programming your National Instruments DAQ hardware, you can use NI application development environment (ADE) software or other ADEs. In either case, you use NI-DAQ.

NI-DAQ

NI-DAQ, which shipped with the NI 6052E, has an extensive library of functions that you can call from your ADE. These functions allow you to use all the features of the NI 6052E.

NI-DAQ carries out many of the complex interactions, such as programming interrupts, between the computer and the DAQ hardware. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you use LabVIEW, Measurement Studio, or other ADEs, your application uses NI-DAQ, as illustrated in Figure 1-1.

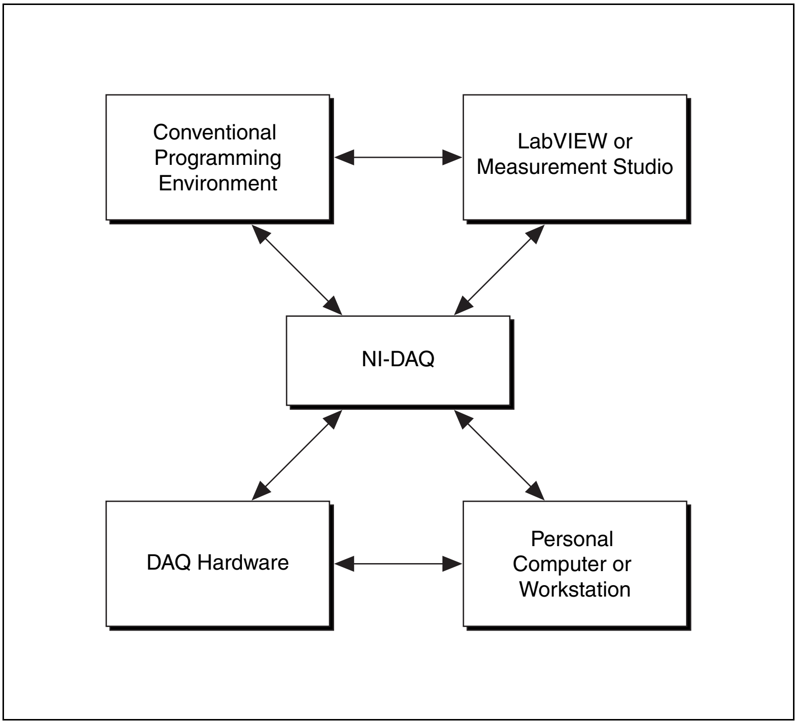


Figure 1-1. The Relationship Between the Programming Environment, NI-DAQ, and the Hardware

To download a free copy of the most recent version of NI-DAQ, click **Download Software** at `ni.com`.

National Instruments ADE Software

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

Measurement Studio, which includes LabWindows/CVI, tools for Visual C++, and tools for Visual Basic, is a development suite that allows you to use ANSI C, Visual C++, and Visual Basic to design your test and measurement software. For C developers, Measurement Studio includes LabWindows/CVI, a fully integrated ANSI C application development environment that features interactive graphics and the LabWindows/CVI Data Acquisition and Easy I/O libraries. For Visual Basic developers, Measurement Studio features a set of ActiveX controls for using National

Instruments DAQ hardware. These ActiveX controls provide a high-level programming interface for building virtual instruments. For Visual C++ developers, Measurement Studio offers a set of Visual C++ classes and tools to integrate those classes into Visual C++ applications. The libraries, ActiveX controls, and classes are available with Measurement Studio and NI-DAQ.

Using LabVIEW or Measurement Studio greatly reduces the development time for your data acquisition and control application.

Optional Equipment

NI offers a variety of products to use with the device, including the following items:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded 50- and 68-pin screw terminals
- RTSI bus cables
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output
- Low channel count signal conditioning modules, devices, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays

For specific information about these products, refer to `ni.com/catalog` or call the office nearest you.

Unpacking

The NI 6052E ships in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge can damage several components on the device.

Caution *Never* touch the exposed pins of connectors.

To avoid damage in handling the device, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the device from the package.

Remove the device from the package and inspect the device for loose components or any sign of damage. Notify NI if the device appears damaged in any way. Do *not* install a damaged device into the computer.

Store the NI 6052E in the antistatic envelope when not in use.

2

Installing and Configuring the NI 6052E

This chapter explains how to install and configure the NI 6052E.

Installing the Software

Install the software before you install the NI 6052E. Install the ADE, such as LabVIEW or Measurement Studio, according to the instructions on the CD and the release notes. After you have installed the ADE, install NI-DAQ according to the instructions on the CD and the *DAQ Quick Start Guide* that is included with the device.

Note It is important to install NI-DAQ before installing the NI 6052E to ensure that the device is properly detected.

Installing the Hardware

You can install the NI PCI/PXI-6052E in any available 5 V PCI or PXI slot, respectively, in the computer. However, to achieve best noise performance, leave as much room as possible between the NI PCI/PXI-6052E and other devices. You can connect the NI DAQPad-6052E for 1394 to any available 1394 port.

The following are general installation instructions. Consult the computer or chassis user manual or technical reference manual for specific instructions and warnings about installing new devices.

Note Follow the guidelines in the computer documentation for installing plug-in hardware.

- NI PCI-6052E
  1. Power off and unplug the computer.
  2. Remove the top cover of the computer.

3. Make sure there are no lighted LEDs on the motherboard. If any are lit, wait until they go out before continuing the installation.
4. Remove the expansion slot cover on the back panel of the computer.
5. Ground yourself using a grounding strap or by holding a grounded object. Follow the ESD protection precautions described in the *Unpacking* section in Chapter 1, *Introduction*.
6. Insert the device into a 5 V PCI slot. Gently rock the device to ease it into place. It can be a tight fit, but *do not force* the device into place.
7. If required, screw the mounting bracket of the NI PCI-6052E to the back panel rail of the computer.
8. Visually verify the installation by ensuring the device is not touching other devices or components and is fully inserted into the slot.
9. Replace the cover.
10. Plug in and power on the computer.

The NI PCI-6052E is now installed.

♦ NI PXI-6052E

1. Power off and unplug the computer.
2. Choose an unused PXI slot in the system. For maximum performance, the NI PXI-6052E has an onboard DMA controller, but you can only use this controller if the device is installed in a slot that supports bus arbitration or bus master cards. NI recommends installing the NI PXI-6052E in such a slot. The PXI specification requires all slots to support bus master cards, but the CompactPCI specification does not. If you install the device in a CompactPCI non-master slot, you must disable the NI PXI-6052E onboard DMA controller using application software.
3. Remove the filler panel for the slot that you chose.
4. Insert the NI PXI-6052E into a 5 V PXI slot. Use the injector/ejector handle to fully insert the device into the chassis.
5. Screw the front panel of the NI PXI-6052E to the front panel mounting rail of the system.
6. Plug in and power on the computer.

The NI PXI-6052E is now installed.

- NI DAQPad-6052E for 1394

Note If you are *not* using the BP-1 battery pack, follow the instructions below. If you are using the BP-1 battery pack, follow the installation instructions in the BP-1 installation guide and disregard step 1 below.

1. Connect the power cord to the wall outlet and to the NI DAQPad-6052E.
2. Connect the 1394 cable from the computer or any other 1394 device to the port on the NI DAQPad-6052E. The computer should immediately detect the NI DAQPad-6052E. When the computer recognizes the NI DAQPad-6052E, the COM LED on the front panel will blink. Refer to the *Configuring the NI 6052E* section of this chapter for information on LEDs.
3. Verify that the power LED is on. Refer to the *Configuring the NI 6052E* section of this chapter for information on LEDs.
4. Configure the device and any accessories with NI-DAQ.

The NI DAQPad-6052E for 1394 is now installed.

You are now ready to configure the hardware and software.

Configuring the NI 6052E

- NI PCI/PXI-6052E

The NI PCI/PXI-6052E is completely software configurable. You must perform two types of configuration on the NI PCI/PXI-6052E—bus-related and data-acquisition-related configuration.

The NI PCI/PXI-6052E is fully compatible with the industry-standard *PCI Local Bus Specification,* Revision 2.2, and *PXI Specification,* Revision 2.0. This compatibility allows the PCI/PXI system to automatically perform all bus-related configurations, including setting the device base memory address and interrupt channel, and requires no user interaction.

You can modify data-acquisition-related configuration settings such as analog input polarity, range, and mode through application-level software, such as NI-DAQ, LabVIEW, and Measurement Studio.

♦ NI DAQPad-6052E for 1394

The NI DAQPad-6052E for 1394 is a completely software-configurable, hot Plug and Play instrument. The Plug and Play services query the instrument and allocate the required resources. The operating system enables the instrument for operation. Refer to the software documentation for more information about Plug and Play.

The NI DAQPad-6052E for 1394 is equipped with two LEDs to help you determine the state of the device:

- Power LED
  - Off—No power is being provided to the device. Either the power cord is unplugged, or the power source is broken.
  - Dim—The device is receiving power but is not connected to an active 1394 port.
  - On—The device is receiving power and is connected to an active 1394 port.
- Communications (COM) LED—The COM LED blinks whenever the device sends or receives any commands or data. This LED should blink once when you first plug in the device. If you are transferring a large amount of data, this light should be on or blinking continually.

Refer to the software documentation for more information on how to configure the device.

3

Hardware Overview

This chapter presents an overview of the hardware functions on the NI 6052E.

Figure 3-1 shows a block diagram for the NI PCI/PXI-6052E.

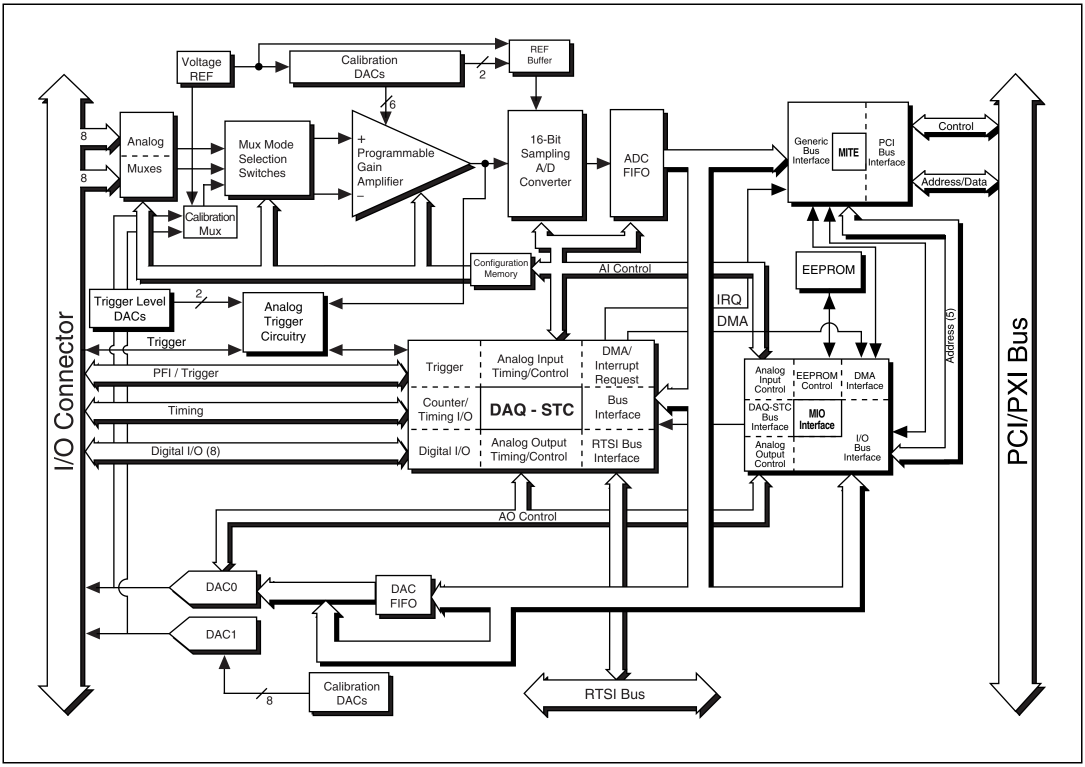


Figure 3-1. PCI and PXI Block Diagram

Figure 3-2 shows a block diagram for the NI DAQPad-6052E.

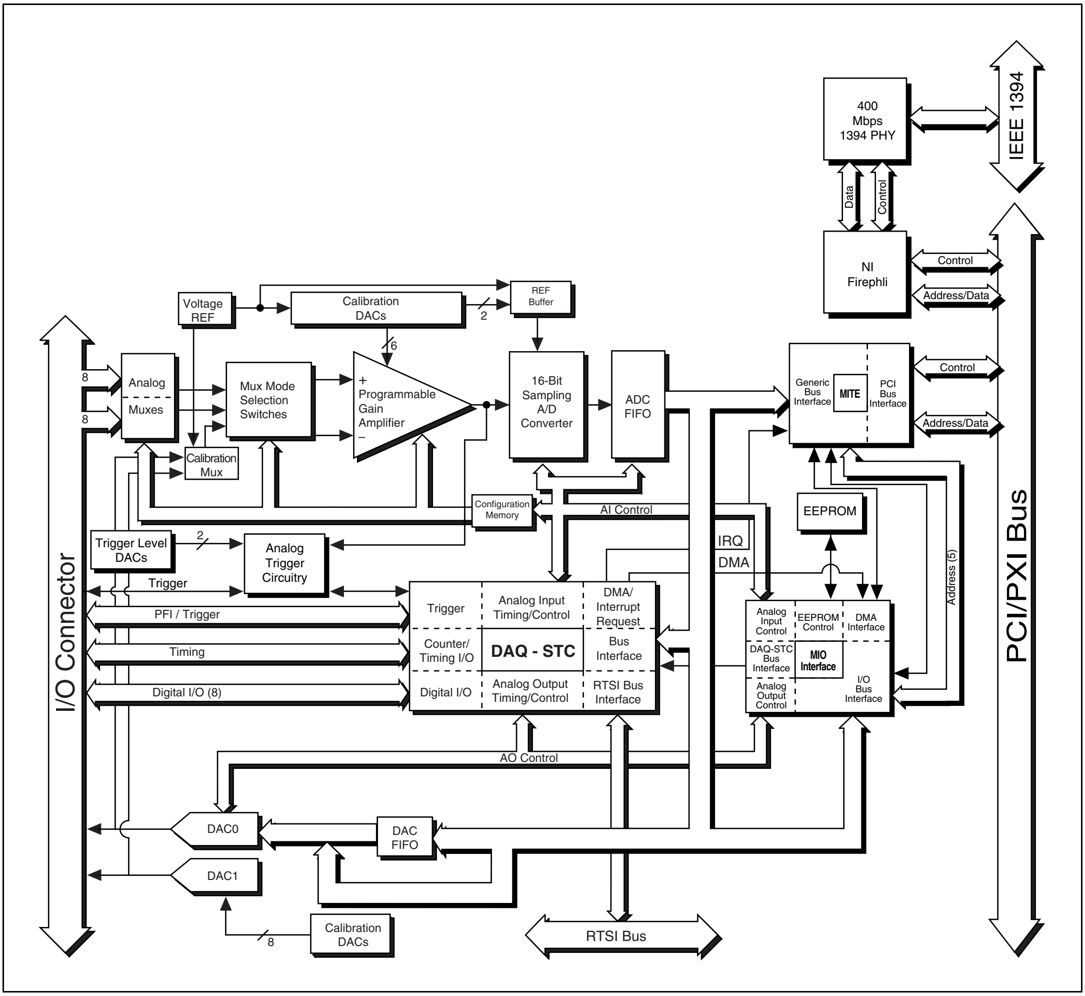


Figure 3-2. NI DAQPad-6052E Block Diagram

Analog Input

The AI section of the NI 6052E is software configurable. You can select different AI configurations through application software designed to control the device. The following sections describe the types of AI configurations.

Input Mode

The NI 6052E has three input modes—nonreferenced single-ended (NRSE) mode, referenced single-ended (RSE) input mode, and differential (DIFF) mode. The NRSE and RSE input modes provide up to 16 channels on the NI 6052E. The DIFF input mode provides up to eight channels on the NI 6052E. Input modes are programmed on a per channel basis for multiple mode scanning. For example, you can configure the circuitry to scan 12 channels—four differentially-configured channels and eight single-ended channels. Table 3-1 describes the three input modes.

Table 3-1. Available Input Modes for the NI 6052E

Configuration	Description
NRSE	A channel configured in NRSE mode uses one analog input line that connects to the positive input of the PGIA. The negative input of the PGIA connects to analog input sense (AISENSE).
RSE	A channel configured in RSE mode uses one analog input line that connects to the positive input of the PGIA. The negative input of the PGIA is internally tied to analog input ground (AIGND).
DIFF	A channel configured in DIFF mode uses two analog input lines. One line connects to the positive input of the device programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA.

For more information about the three input modes, refer to the *Analog Input Signal Connections* section in Chapter 4, *Connecting the Signals*, which contains signal-path diagrams for the three modes.

Input Polarity and Input Range

The NI 6052E has two input polarities—unipolar and bipolar. Unipolar input polarity means that the input voltage range is between 0 and V_{ref}, where V_{ref} is a positive reference voltage. Bipolar input polarity means that the input voltage range is between $-V_{ref}/2$ and $+V_{ref}/2$. The device has a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 10 V (±5 V).

Polarity and range settings can be programmed on a per channel basis so that you can uniquely configure each input channel.

The software-programmable gains on the NI 6052E increase the overall flexibility of the device by matching the input signal ranges to those that the ADC can accommodate. Each device has gains of 0.5, 1, 2, 5, 10, 20, 50, and 100 and is suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-2 shows the overall input range and precision according to the input-range configuration and gain used.

Table 3-2. Actual Range and Measurement Precision

Range Configuration	Gain	Actual Input Range	Precision*
0 to +10 V	1.0	0 to +10 V	153 µV
	2.0	0 to +5 V	76.3 µV
	5.0	0 to +2 V	30.5 µV
	10.0	0 to +1 V	15.3 µV
	20.0	0 to +500 mV	7.63 µV
	50.0	0 to +200 mV	3.05 µV
	100.0	0 to +100 mV	1.53 µV
–5 to +5 V	0.5	–10 to +10 V	305 µV
	1.0	–5 to +5 V	153 µV
	2.0	–2.5 to +2.5 V	76.3 µV
	5.0	–1 to +1 V	30.5 µV
	10.0	–500 to +500 mV	15.6 µV
	20.0	–250 to +250 mV	7.63 µV
	50.0	–100 to +100 mV	3.05 µV
	100.0	–50 to +50 mV	1.53 µV

* The value of 1 least significant bit (LSB) of the 16-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 16-bit count.

Note: Refer to Appendix A, *Specifications*, for absolute maximum ratings.

Considerations for Selecting Input Ranges

The input polarity and range you select depends on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution, but it can result in the input signal going out of range. For best results, match the input range as closely as possible to the expected range of the input signal. For example, if you are certain the input signal is not below 0 V, use unipolar input polarity. If the signal is negative, however, you get inaccurate readings using unipolar input polarity.

Multiple-Channel Scanning Considerations

The NI 6052E can sample multiple channels at the same maximum rate as the single-channel rate; however, pay careful attention to the *settling time*. Settling time is the time required for an amplifier, relays, or other circuits to reach a stable mode of operation. The settling time is independent of the selected gain, even at the maximum sampling rate. The settling time for very high-speed devices is gain dependent, which can affect the useful sampling rate for a given gain. However, as long as the gain is constant and source impedances are low, no extra settling time is necessary between channels. Refer to Appendix A, *Specifications*, for a complete list of settling times.

Settling times can increase when scanning channels with various gains. When the programmable gain instrumentation amplifier (PGIA) switches to a higher gain, the signal on the previous channel can be well outside the new, smaller range. For example, suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1, and the PGIA is programmed to apply a gain of 1 to channel 0 and a gain of 100 to channel 1. When the multiplexer switches to channel 1 and the PGIA switches to a gain of 100, the new full-scale range is 100 mV (if the ADC is in unipolar mode). The 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. For a 16-bit device to settle within 0.0015% (15 ppm or 1 LSB) of the full-scale range on channel 1, the input circuitry must settle within 0.00004% (0.4 ppm or 1/400 LSB) of the 4 V step. The circuitry may take up to 200 µs to settle this much. In general, this extra settling time is unneeded when the PGIA is switching to a lower gain.

A phenomenon called *charge injection*, in which the AI multiplexer injects a small amount of charge into each signal source when that source is selected, can cause settling times to increase when scanning high-impedance signals. If the impedance of the source is too high, the effect of the charge—a voltage error—will not have decayed by the time the ADC samples the signal. For this reason, keep source impedances under 1 kΩ to perform high-speed scanning.

Due to problems with settling times, multiple-channel scanning is not recommended unless sampling rates are low or you must sample several signals almost simultaneously. The data is much more accurate and channel-to-channel independent if you acquire data independently from each channel (for example, 100 points from channel 0, then 100 points from channel 1, then 100 points from channel 2, and so on).

Analog Output

The NI 6052E supplies two channels of AO voltage at the I/O connector. The reference and range for the analog output circuitry is software configurable. The reference can be either internal or external, and the range can be either bipolar or unipolar.

Analog Output Reference Selection

You can connect each DAC to an internal reference of 10 V or to the external reference signal connected to the EXTREF pin on the I/O connector. The signal applied to EXTREF should be within ±11 V. You do not need to configure both channels to use the same reference.

Analog Output Polarity Selection

You can configure each AO channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to V_{ref} at the analog output. A bipolar configuration has a range of $-V_{ref}$ to $+V_{ref}$ at the analog output. V_{ref} is the voltage reference used by the DACs in the analog output circuitry and can be either the +10 V onboard reference or an externally supplied reference within ±11 V. You do not need to configure both channels for the same range.

Selecting a bipolar range for a particular DAC means that any data written to that DAC is interpreted in two's-complement mode. In two's-complement mode, data values written to the AO channel can be either positive or negative. If you select unipolar range, data is interpreted in straight binary mode. In straight binary mode, data values written to the AO channel range must be positive.

Analog Output Reglitch

In normal operation, a DAC output glitches when it is updated with a new value. The glitch energy differs from code to code and appears as distortion in the frequency spectrum. Each analog output contains a reglitch circuit that generates uniform glitch energy at every code rather than large glitches at major code transitions. This uniform glitch energy appears as a multiple of the update rate in the frequency spectrum. This reglitch circuit does *not* eliminate the glitches; it only makes them more uniform in size.

Analog Trigger

In addition to supporting internal software triggering and external digital triggering to initiate a DAQ sequence, the NI 6052E also supports analog triggering. You can configure the analog trigger circuitry to accept either a direct analog input from the PFI0/TRIG1 pin on the I/O connector or a postgain signal from the output of the PGIA, as shown in Figure 3-3. The trigger-level range for the direct analog channel is in 4.9 mV steps. The range for the post-PGIA trigger selection is the full-scale range of the selected channel. The resolution is that range divided by 4,096.

Note The PFI0/TRIG1 pin is an analog input when configured as an analog trigger. Therefore, it is susceptible to crosstalk from adjacent pins, resulting in false triggering when the pin is unconnected. To avoid false triggering, ensure that this pin is connected to a low-impedance signal source (less than 1 kΩ source impedance) if you plan to enable this input using the application software.

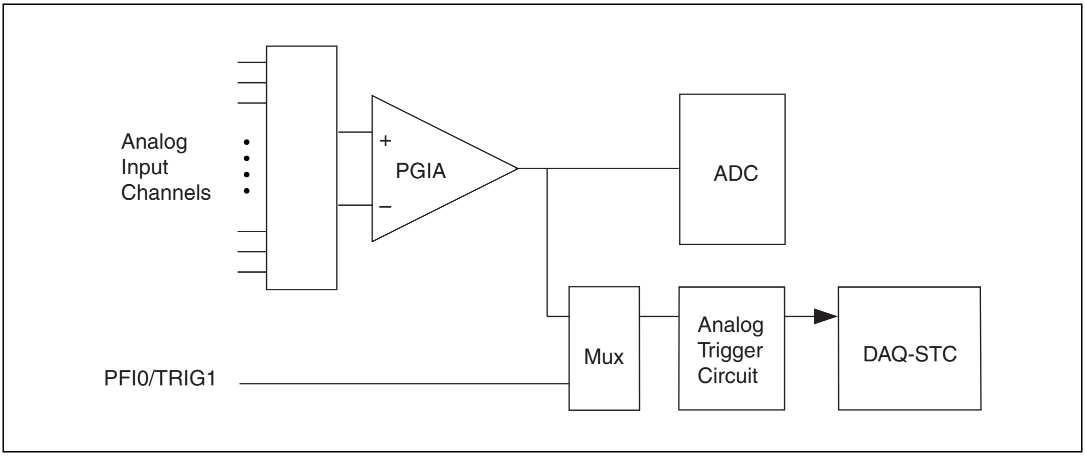


Figure 3-3. Analog Trigger Block Diagram

Five analog triggering modes are available, as shown in Figures 3-4 to 3-8. You can independently set **lowValue** and **highValue** in your ADE.

In below-low-level analog triggering mode, the trigger is generated when the signal value is less than **lowValue**. **HighValue** is not used.

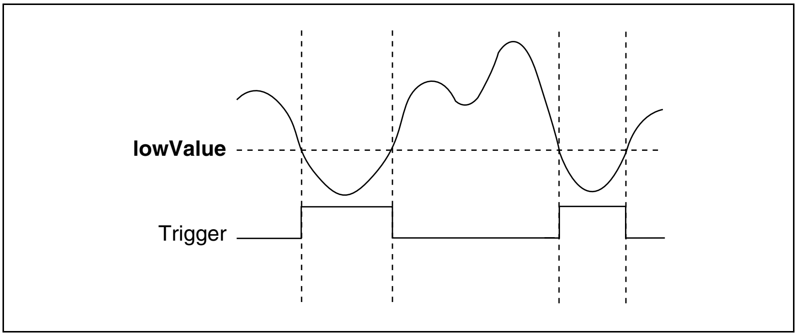


Figure 3-4. Below-Low-Level Analog Triggering Mode

In above-high-level analog triggering mode, the trigger is generated when the signal value is greater than **highValue**. **LowValue** is not used.

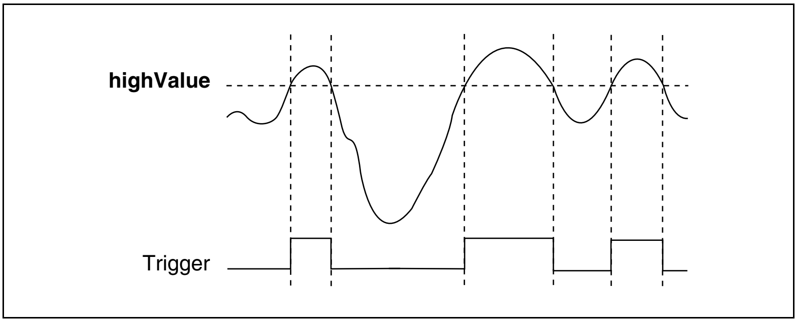


Figure 3-5. Above-High-Level Analog Triggering Mode

In inside-region analog triggering mode, the trigger is generated when the signal value is between the **lowValue** and the **highValue.**

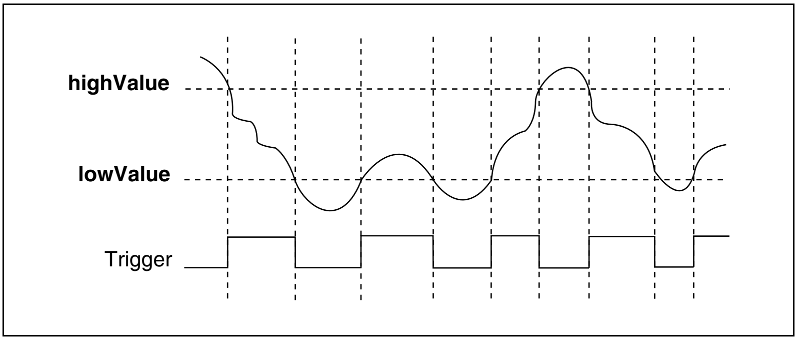


Figure 3-6. Inside-Region Analog Triggering Mode

In high-hysteresis analog triggering mode, the trigger is generated when the signal value is greater than **highValue**, with the hysteresis specified by **lowValue**.

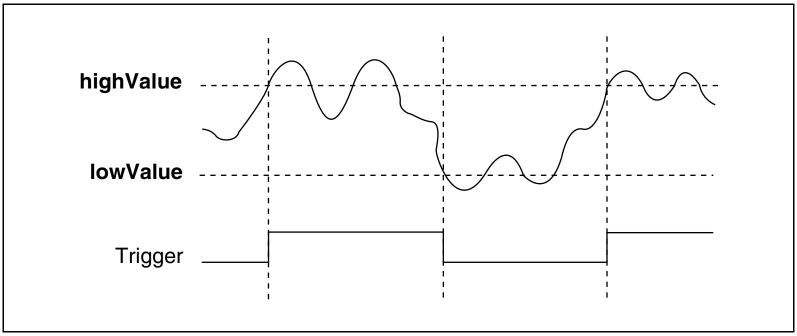


Figure 3-7. High-Hysteresis Analog Triggering Mode

In low-hysteresis analog triggering mode, the trigger is generated when the signal value is less than **lowValue**, with the hysteresis specified by **highValue**.

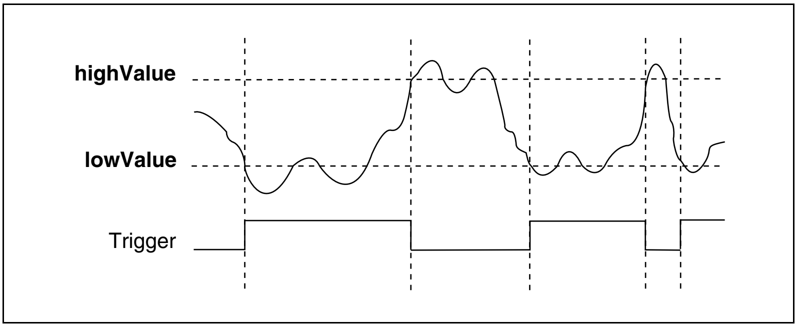


Figure 3-8. Low-Hysteresis Analog Triggering Mode

The analog trigger circuit generates an internal digital trigger based on the AI signal and the user-defined trigger levels. This digital trigger can be used by any of the three timing sections of the DAQ-STC. For example, the AI section can be configured to acquire *n* scans after the AI signal crosses a specific threshold. The AO section can be configured to update its outputs whenever the AI signal crosses a specific threshold.

Digital I/O

The NI 6052E contains eight lines of DIO for general-purpose use. Each line is software programmable for either input or output. At system startup and reset, the DIO ports are all high-impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the counters. The up/down control signals are input-only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a flexible interface for connecting timing signals to other devices or external circuitry. The NI 6052E uses the RTSI bus to interconnect timing signals between devices and the Programmable Function Input (PFI) pins on the I/O connector to connect the device to external circuitry. These connections are designed to enable the device to both control and be controlled by other devices and circuits.

The DAQ-STC has 13 internal timing signals you can control by an external source. These timing signals can also be controlled by signals internally generated to the DAQ-STC, and these selections are software configurable. Figure 3-9 shows an example of the signal routing multiplexer controlling the CONVERT* signal.

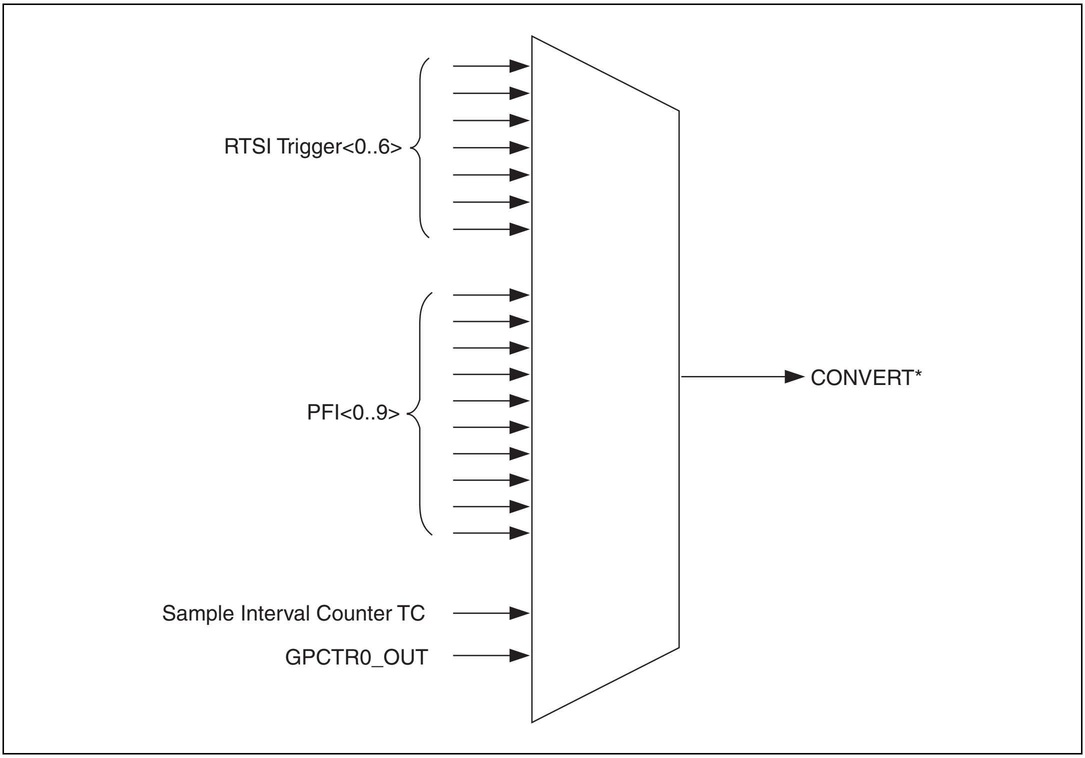


Figure 3-9. CONVERT* Signal Routing

Figure 3-9 shows that CONVERT* can be generated from a number of sources, including the external signals RTSI<0..6> and PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available as outputs on the RTSI pins, as indicated in the *RTSI Triggers* section, and on the PFI pins, as indicated in Chapter 4, *Connecting the Signals*.

Programmable Function Inputs

Ten PFI signals connect to the signal routing multiplexer for each timing signal, and software can select any PFI pin as the external source for a given timing signal. Any PFI pin can be used as an input by any timing signal, and multiple timing signals can simultaneously use the same PFI. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications. You can also individually enable each PFI pin to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, the software can turn on the output driver for the PFI5/UPDATE* pin.

Device and RTSI Clocks

Many functions performed by the NI 6052E require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector.

The NI 6052E can use either its internal 20 MHz timebase or a timebase received over the RTSI bus on the RTSI Clock line. This timebase is software configurable. If you configure the device to use the internal timebase, you can program the device to drive its internal timebase over the RTSI bus to another device programmed to receive this timebase signal. This clock source, whether local or from the RTSI bus, is used directly by the device as the primary frequency source. The default configuration is to use the internal timebase without driving the RTSI bus timebase signal. The NI PCI-6052E has separate connectors for the RTSI bus. The NI PXI-6052E uses signals on the PXI backplane for the RTSI Clock. The RTSI Clock signal uses the PXI trigger<7> line for this connection.

RTSI Triggers

The RTSI trigger lines on the RTSI bus provide a flexible interconnection scheme for any NI 6052E that shares the RTSI bus. The NI PCI-6052E has seven trigger lines. These bidirectional lines can drive any of eight timing signals onto the RTSI bus and can receive any of these timing signals. Figure 3-10 shows the PCI signal connection scheme.

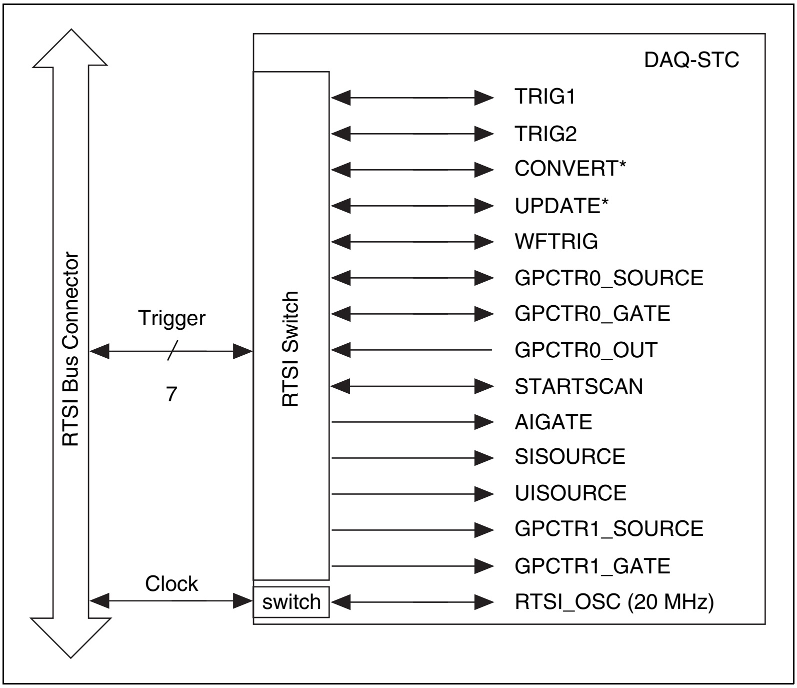


Figure 3-10. NI PCI-6052E RTSI Bus Signal Connection

For the NI PXI-6052E, the RTSI trigger lines connect to other devices through the PXI bus on the PXI backplane. RTSI<0..5> connects to PXI Trigger<0..5>, and RTSI<6> connects to PXI Star. Figure 3-11 shows this signal connection scheme.

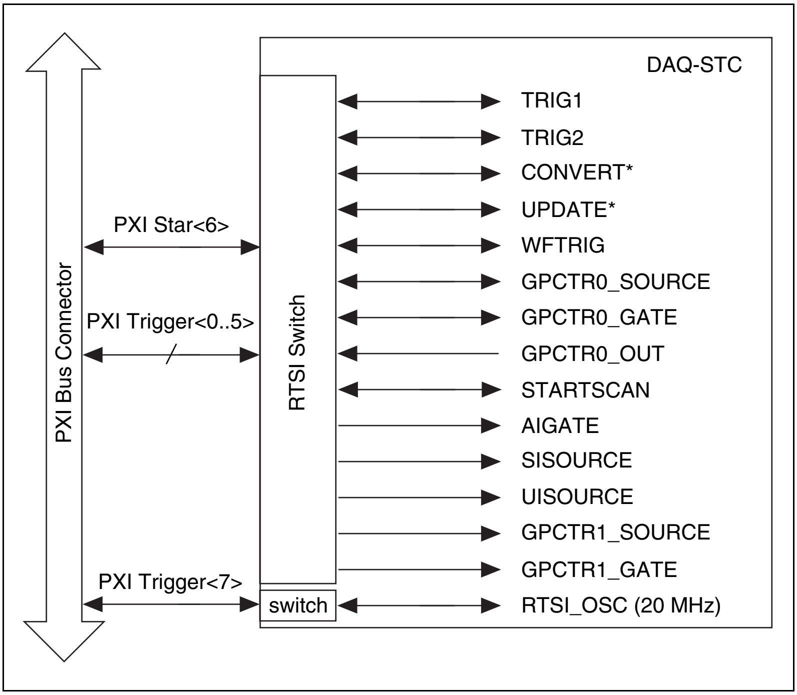


Figure 3-11. NI PXI-6052E RTSI Bus Signal Connection

The four RTSI trigger lines on the RTSI bus provide a flexible interconnection scheme for any NI DAQPad-6052E sharing the RTSI bus. The NI DAQPad-6052E has four trigger lines. These bidirectional lines can drive any of eight timing signals onto the RTSI bus and can receive any of these timing signals. This signal connection scheme is shown in Figure 3-12.

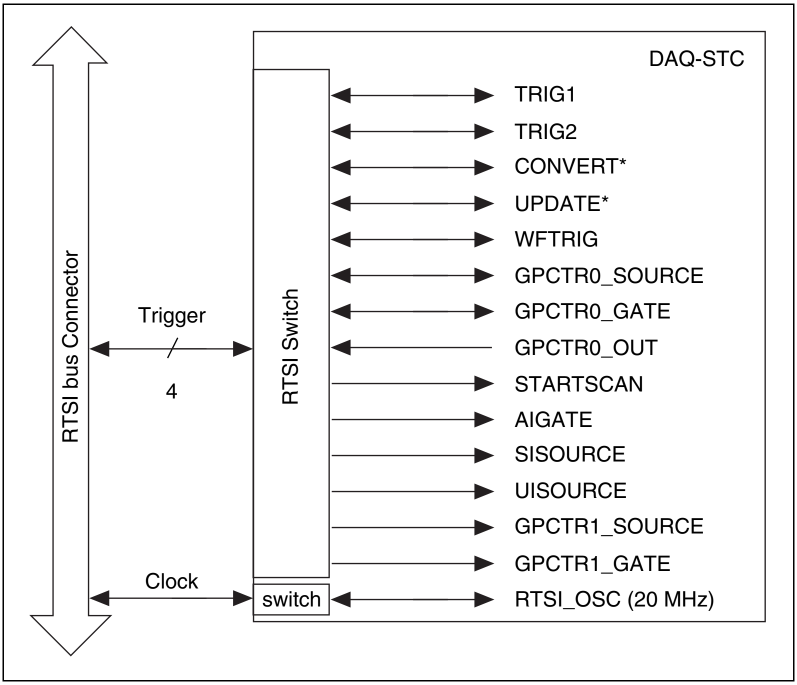


Figure 3-12. NI DAQPad-6052E RTSI Bus Signal Connection

Refer to the *Connecting Timing Signals* section in Chapter 4, *Connecting the Signals*, for a description of the signals shown in Figures 3-10, 3-11, and 3-12.

4

Connecting the Signals

This chapter describes how to make input and output signal connections to the device using the device I/O connector.

The I/O connector has 68 pins on the NI 6052E that you can connect to 68-pin accessories with the SH6868 shielded cable or the R6868 ribbon cable. You can connect the device to 50-pin signal conditioning modules and terminal blocks with the SH6850 shielded cable or R6850 ribbon cable.

The NI DAQPad-6052E with BNCs provides easy-to-use user I/O directly on the front of the box. Analog input, analog output, CTR0 Out, PFI0, and External Reference are accessible through BNCs. You can use USER1 and USER2 to convert a signal on a BNC cable to a signal wire on the connector block. This conversion makes connecting a BNC cable to a PFI/Trigger pin easier. The rest of the signals are accessible through a removable screw terminal block. Extra removable terminal blocks are available.

Besides the standard I/O connections, both versions of the NI DAQPad-6052E have RTSI and an analog expansion bus for connecting to SCXI.

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector.

Refer to Appendix B, *Custom Cabling and Optional Connectors*, for the pin assignments of the 50-pin connector. Refer to Table 4-1 for signal descriptions.

Signal	Pin	Pin	Signal
ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT	22	56	AIGND
DAC1OUT	21	55	AOGND
EXTREF	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

Figure 4-1. I/O Connector Pin Assignment for the NI 6052E

Figure 4-2 shows the pin assignments for the front panel I/O connections on the NI DAQPad-6052E with BNCs. Refer to Table 4-1 for signal descriptions.

Signal	Pin	Pin	Signal
PFI 9	2	1	DIO 7
PFI 8	4	3	DIO 6
PFI 7	6	5	DIO 5
PFI 6	8	7	DIO 4
PFI 5	10	9	DIO 3
PFI 4	12	11	DIO 2
PFI 3	14	13	DIO 1
PFI 2	16	15	DIO 0
PFI 1	18	17	CTR 1 OUT
DGND	20	19	DGND
USER 2	22	21	USER 1
FRQ OUT	24	23	SCAN CLK
+5 V	26	25	EXT STRB
+5 V	28	27	AISENSE
DGND	30	29	AIGND

Figure 4-2. I/O Connector Pin Assignment for the NI DAQPad-6052E with BNCs

Table 4-1 lists the signal names, gives the signal references and directions, and describes all the signals for the NI 6052E.

Table 4-1. I/O Connector Signal Descriptions

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements in RSE configuration and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected on the device.
ACH<0..15>	AIGND	Input	Analog Input Channels 0 through 15—Each channel pair, ACH <*i, i* + 8> (*i* = 0..7), can be configured as either one differential input or two single-ended inputs.
ACH<16..63>	AIGND	Input	Analog Input Channels 16 through 63 (NI 6053E only)—Each channel pair, ACH <*i*, *i* + 8> (i=16..23, 32..39, 48..55) can be configured as either one differential input or two single-ended inputs.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for any of channels ACH <0..15> in NRSE configuration.
DAC0OUT	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of analog output channel 0.

Table 4-1. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
DAC1OUT	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of analog output channel 1.
EXTREF	AOGND	Input	External Reference—This input is the external reference input for the analog output circuitry.
AOGND	—	—	Analog Output Ground—The analog output voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected on the NI 6052E.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector and the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected on the NI 6052E.
DIO<0..7>	DGND	Input or Output	Digital I/O signals—DIO 6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5 V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion in the scanning modes when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.
PFI0/TRIG1	DGND	Input Output	PFI0/Trigger 1—As an input, this is either one of the PFIs or the source for the hardware analog trigger. PFI signals are explained in the *Connecting Timing Signals* section. The hardware analog trigger is explained in the *Analog Trigger* section in Chapter 3, *Hardware Overview*. As an output, this is the TRIG1 signal. In posttrigger data acquisition sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input Output	PFI1/Trigger 2—As an input, this is one of the PFIs. As an output, this is the TRIG2 signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.

Table 4-1. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
PFI2/CONVERT*	DGND	Input Output	PFI2/Convert—As an input, this is one of the PFIs. As an output, this is the CONVERT* signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input Output	PFI3/Counter 1 Source—As an input, this is one of the PFIs. As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input Output	PFI4/Counter 1 Gate—As an input, this is one of the PFIs. As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input Output	PFI5/Update—As an input, this is one of the PFIs. As an output, this is the UPDATE* signal. A high-to-low edge on UPDATE* indicates that the analog output primary group is being updated.
PFI6/WFTRIG	DGND	Input Output	PFI6/Waveform Trigger—As an input, this is one of the PFIs. As an output, this is the WFTRIG signal. In timed analog output sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input Output	PFI7/Start of Scan—As an input, this is one of the PFIs. As an output, this is the STARTSCAN signal. This pin pulses once at the start of each analog input scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input Output	PFI8/Counter 0 Source—As an input, this is one of the PFIs. As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input Output	PFI9/Counter 0 Gate—As an input, this is one of the PFIs. As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.

Table 4-1. I/O Connector Signal Descriptions (Continued)

Signal Name	Reference	Direction	Description
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

Each analog input for the NI DAQPad-6052E with BNCs has a switch that you set based on whether the BNC is connected to a floating source (FS) or a grounded source (GS). Figure 4-3 shows how setting the switch to FS connects the negative terminal of the differential input to ground through a 5 kΩ in parallel with 0.1 µF resistor. If you are using a differential channel connected to a floating source, set the switch to FS. Set the switch to GS to allow both positive and negative terminals to float. If you are using a single-ended channel or using a differential channel connected to a grounded source, set the switch to GS. Refer to the *Types of Signal Sources* section for more information on single-ended channels, differential channels, floating sources, and grounded sources.

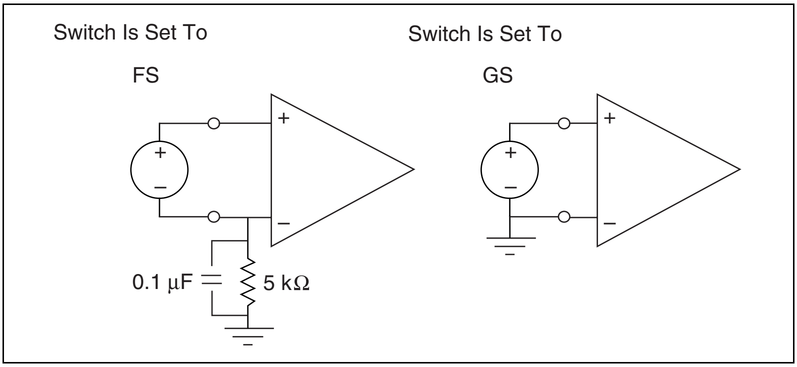


Figure 4-3. Floating Source and Grounded Source Connections

External Expansion Connector

The external expansion connector is located on the back panel of the NI DAQPad-6052E. You use this connector to connect to SCXI in serial mode. Using the external expansion connector does not use any analog input channels but does use DIO0, DIO1, DIO2, DIO4, and PF17/STARTSCAN.

Caution Connections that exceed any of the maximum ratings of input or output signals on the NI 6052E can damage the device and the computer. Maximum input ratings for each signal are given in the *Protection* column of Table 4-2. NI is *not* liable for any damage resulting from such signal connections.

Table 4-2. I/O Signal Summary

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..63>	AI	100 GΩ in parallel with 100 pF	±25/15	—	—	—	±200 pA
AISENSE, AISENSE2	AI	100 GΩ in parallel with 100 pF	±25/15	—	—	—	±200 pA
AIGND	AO	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	20 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	20 V/µs	—
EXTREF	AI	10 kΩ	±25/15	—	—	—	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1A at 5	—	—	—
DIO<0..7>	DIO	—	V_{cc} + 0.5	13 at (V_{cc} – 0.4)	24 at 0.4	1.1	50 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	AI DIO	10 kΩ	±35 V_{cc} + 0.5	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	9 kΩ pu and 10 kΩ pd
PFI1/TRIG2	DIO	—	V_{cc} + 0.5	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} + 0.5	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} + 0.5	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} + 0.5	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} + 0.5	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-2. I/O Signal Summary (Continued)

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI6/WFTRIG	DIO	—	V_{cc} + 0.5	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} + 0.5	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} + 0.5	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} + 0.5	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc} – 0.4)	5 at 0.4	1.5	50 kΩ pu

AI = Analog Input
AO = Analog Output
AI/DIO = Analog/Digital Input/Output
DIO = Digital Input/Output
DO = Digital Output
pu = pullup
pd = pulldown

* Indicates active low

Note: The tolerance on the 50 kΩ pullup and pulldown resistors is very large. Actual value can range between 17 kΩ and 100 kΩ.

PXI-specific features are implemented on the J2 connector of the CompactPCI bus. Table 4-3 shows the J2 pins used by the NI PXI-6052E. The device is compatible with any CompactPCI chassis with a sub-bus that does not drive these lines. However, if the sub-bus is capable of driving these lines, the device is only compatible if those pins on the sub-bus are disabled by default and are never enabled. Damage can result if these lines are driven by the sub-bus.

Table 4-3. Pins Used by the NI PXI-6052E

NI PXI-6052E Signal	PXI Pin Name	PXI J2 Pin Number
RTSI<0..5>	PXI Trigger<0..5>	B16, A16, A17, A18, B18, C18
RTSI 6	PXI Star	D17
RTSI Clock	PXI Trigger 7	E16
Reserved	LBL<0..3>	C20, E20, A19, C19
Reserved	LBR<0..12>	A21, C21, D21, E21, A20, B20, E15, A3, C3, D3, E3, A2, B2

Analog Input Signal Connections

The AI signals are ACH<0..15>, AISENSE, and AIGND. The ACH<0..15> signals are connected to the 16 AI channels of the NI 6052E. In single-ended modes, signals connected to ACH<0..15> are routed to the positive input of the PGIA. In DIFF mode, signals connected to ACH<0..7> are routed to the positive input of the PGIA, and signals connected to ACH<8..15> are routed to the negative input of the PGIA.

Caution Exceeding the differential and common-mode input ranges distorts the input signals. Exceeding the maximum input voltage rating can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections. The maximum input voltage ratings are listed in the *Protection* column of Table 4-2.

In NRSE mode, the AISENSE signal is internally connected to the negative input of the PGIA when the corresponding channels are selected. In DIFF and RSE modes, the signal is left unconnected.

AIGND is an AI common signal that is routed directly to the ground tie point on the device. You can also use this signal for a general analog ground tie point to the device.

Connect the AI signals to the device according to the configuration of the AI channels you are using and the type of input signal source. With each configuration, you can use the PGIA in a different way. Figure 4-4 shows a diagram of the PGIA.

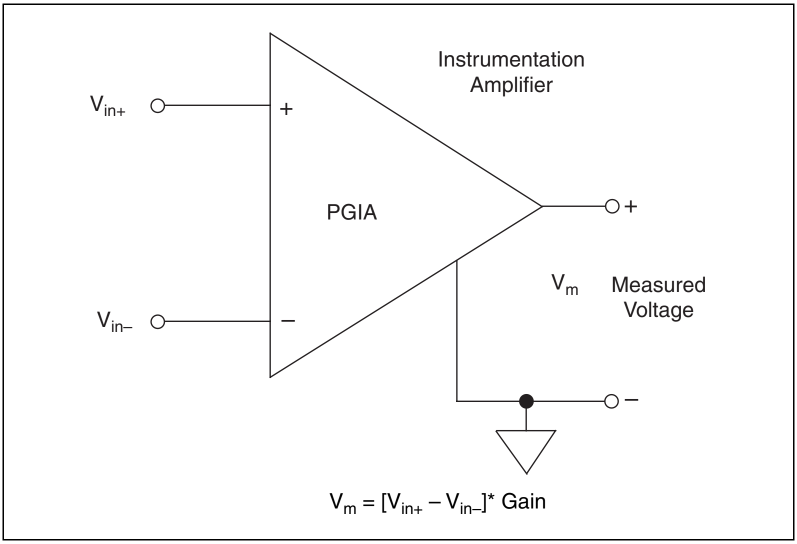


Figure 4-4. PGIA

The PGIA applies gain and common-mode voltage rejection and presents high-input impedance to the AI signals connected to the device. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the device. The PGIA converts two input signals to a signal that equals the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the ground for the device. The ADC measures this output voltage when it performs A/D conversions.

You must reference all signals to ground either at the signal source or at the device. If you have a floating source, reference the signal to ground by using the RSE input mode or the DIFF input mode with bias resistors. Refer to the *Differential Connections for Nonreferenced or Floating Signal Sources* section for more information. If you have a grounded source, do not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input modes.

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these signal types.

Floating Signal Sources

A floating signal source is not connected to the building ground system. Instead, it has an isolated ground-reference point. An instrument or device that has an isolated output is a floating signal source. Some floating signal source examples are the outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. You must tie the ground reference of a floating signal to the device analog input ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats from the common-mode input range.

Ground-Referenced Signal Sources

A ground-referenced signal source is connected to the building system ground. Therefore, it is already connected to a common ground point with respect to the device, assuming that the computer is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

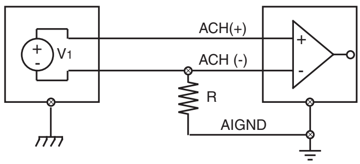
The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are improperly connected. If a ground-referenced signal source is improperly measured, this difference can appear as a measurement error. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

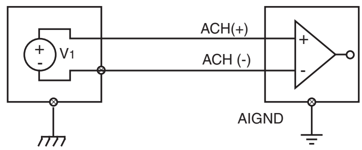
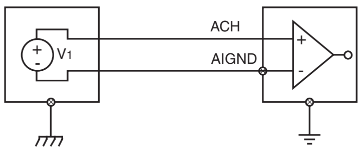
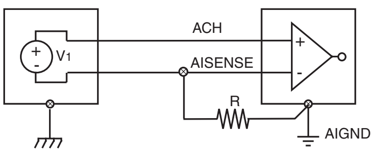
Input Configurations

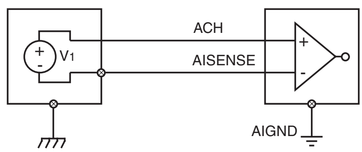
The following sections discuss the use of single-ended and differential input modes and considerations for measuring both floating and ground-referenced signal sources.

Table 4-4 summarizes the recommended input configuration for both types of signal sources.

Table 4-4. Summary of Analog Input Connections

<table>
<tr><th rowspan="3">Input</th><th colspan="2">Signal Source Type</th></tr>
<tr><th>Floating Signal Source
(Not Connected to Building Ground)</th><th>Grounded Signal Source</th></tr>
<tr><td>Examples
• Ungrounded thermocouples
• Signal conditioning with isolated outputs
• Battery devices</td><td>Examples
Plug-in instruments with nonisolated outputs</td></tr>
<tr><td>Differential
(DIFF)</td><td>

Refer to the Differential Connections for Nonreferenced or Floating Signal Sources section for more information about bias resistors.</td><td>
</td></tr>
<tr><td>Single-Ended
Ground
Referenced
(RSE)</td><td>
</td><td>This configuration is not recommended.</td></tr>
<tr><td>Single-Ended
Nonreferenced
(NRSE)</td><td>

Refer to the Differential Connections for Nonreferenced or Floating Signal Sources section for more information about bias resistors.</td><td>
</td></tr>
</table>

Differential Connection Considerations (DIFF Input Configuration)

In a differential connection, the device AI signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF input mode. The input signal is connected to the positive input of the PGIA. The reference signal, or return, is connected to the negative input of the PGIA.

When you configure a channel for differential input, each signal uses two multiplexer inputs—one for the signal and one for the reference signal. Therefore, with a differential configuration for every channel, up to eight AI channels are available. Use differential input connections for any signal that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the NI 6052E are greater than 10 ft (3 m).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce noise pickup and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-5 shows how to connect a floating signal source to a channel on the NI 6052E configured in DIFF input mode.

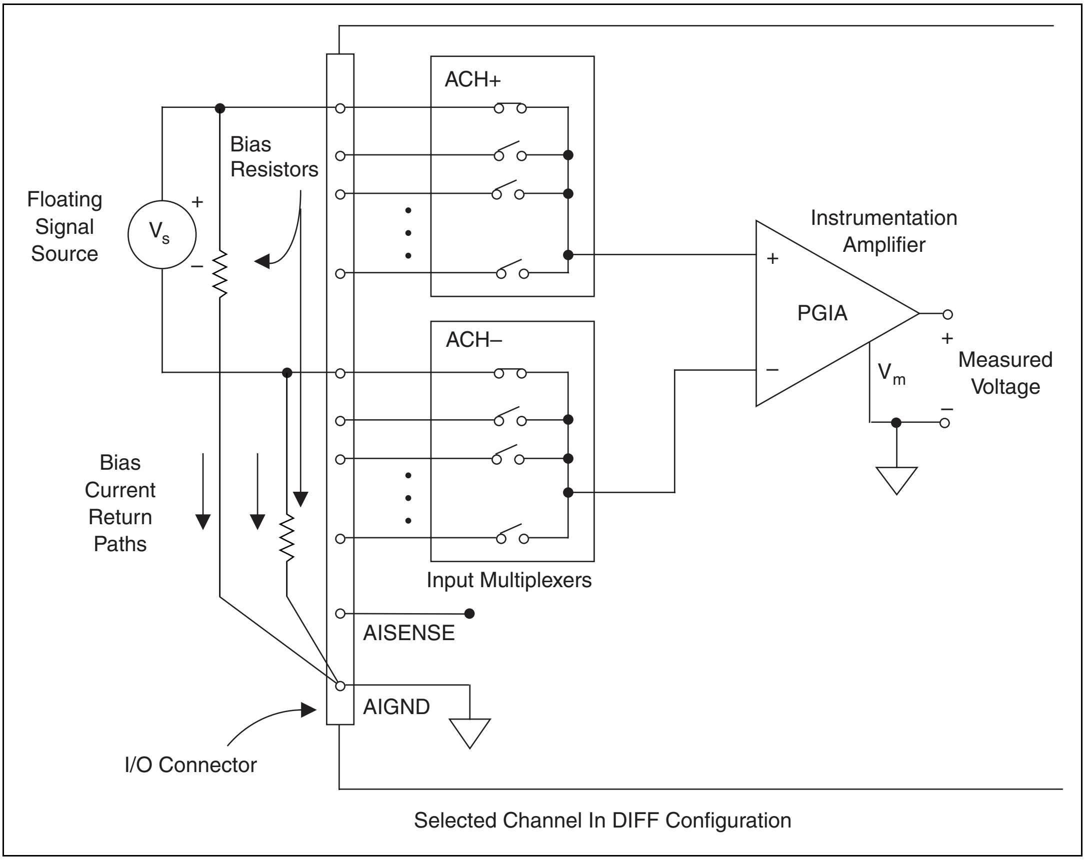


Figure 4-5. Differential Input Connections for Nonreferenced Signals

Figure 4-5 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is unlikely to remain within the common-mode signal range of the PGIA. The PGIA will then saturate, causing erroneous readings. To avoid this error, you must reference the source to AIGND by connecting the positive side of the signal to the positive input of the PGIA and connecting the negative side of the signal to AIGND as well as to the negative input of the PGIA, without any resistors.

This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the differential signal path significantly off balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Thus, this noise appears as a differential-mode signal instead of a common-mode signal, and the PGIA does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so nearly similar amounts of noise couple onto both connections, yielding better rejection of electrostatically coupled noise. Also, this configuration does not load down the source (other than the high-input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 4-5. This balanced configuration offers slightly better noise rejection, but it loads down the source with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the PGIA require a DC path to ground for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AIGND. If the source has low impedance, choose a resistor that is large enough not to significantly load the source, but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, you can connect the negative input directly to AIGND. If the source has high output impedance, you should balance the signal path as previously described, using the same value resistor on both the positive and negative inputs. Some gain error is produced by loading down the source.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-6 shows how to connect a ground-referenced signal source to a channel on the NI 6052E configured in DIFF input mode.

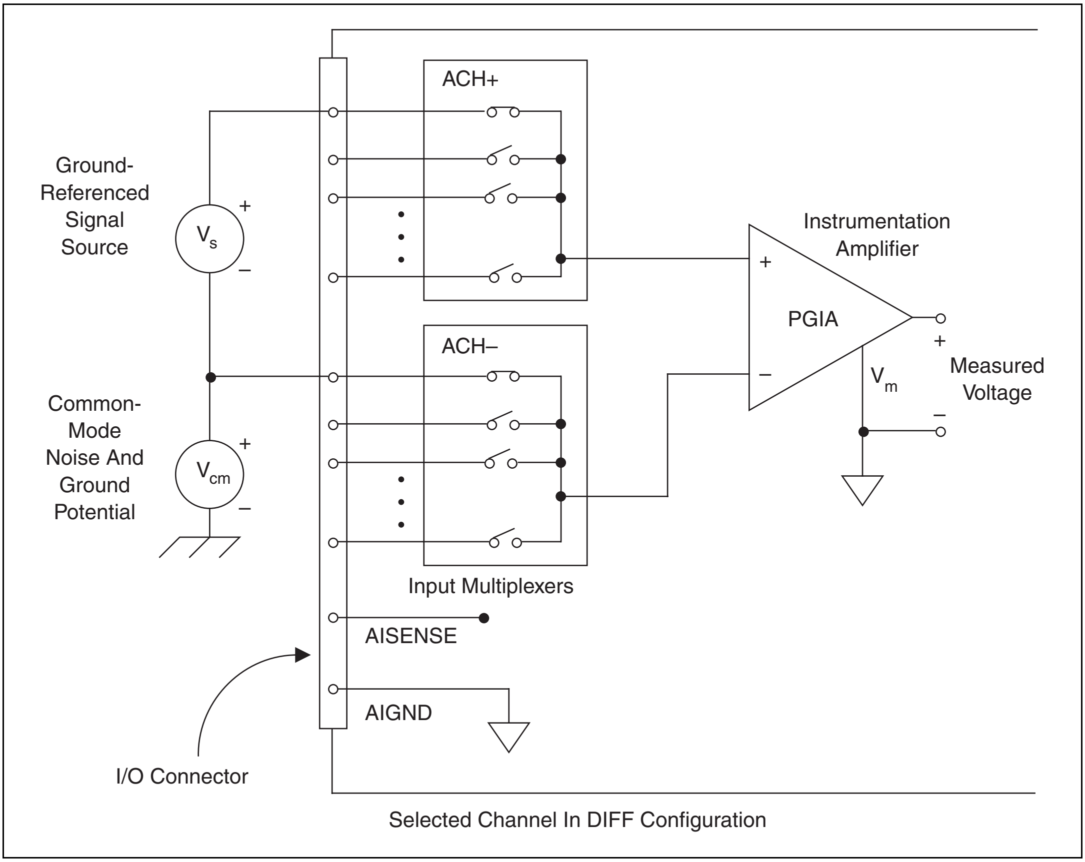


Figure 4-6. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground, shown as V_{cm} in Figure 4-6.

Single-Ended Connection Considerations

In a single-ended connection, the analog input signal is referenced to a ground that can be shared with other input signals. The input signal is connected to the positive input of the PGIA, and the ground is connected to the negative input of the PGIA.

When every channel is configured for single-ended input, up to 16 AI channels on the NI 6052E are available. Use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high level (greater than 1 V).
- The leads connecting the signal to the device are less than 10 ft (3 m).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for input signals that do not meet the preceding conditions.

Using application software, you can configure the NI 6052E channels for RSE or NRSE input mode. The RSE configuration is used for floating signal sources. In this case, the NI 6052E provides the reference ground point for the external signal. The NRSE configuration is used for ground-referenced signal sources. In this case, the external signal supplies its own reference ground point. The device should not supply one.

In single-ended configurations, more electrostatic and magnetic noise couples into the signal connections than in the DIFF configuration. The coupling is a result of signal path differences. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two signal conductors.

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 4-7 shows how to connect a floating signal source to a channel on the NI 6052E configured for RSE input mode.

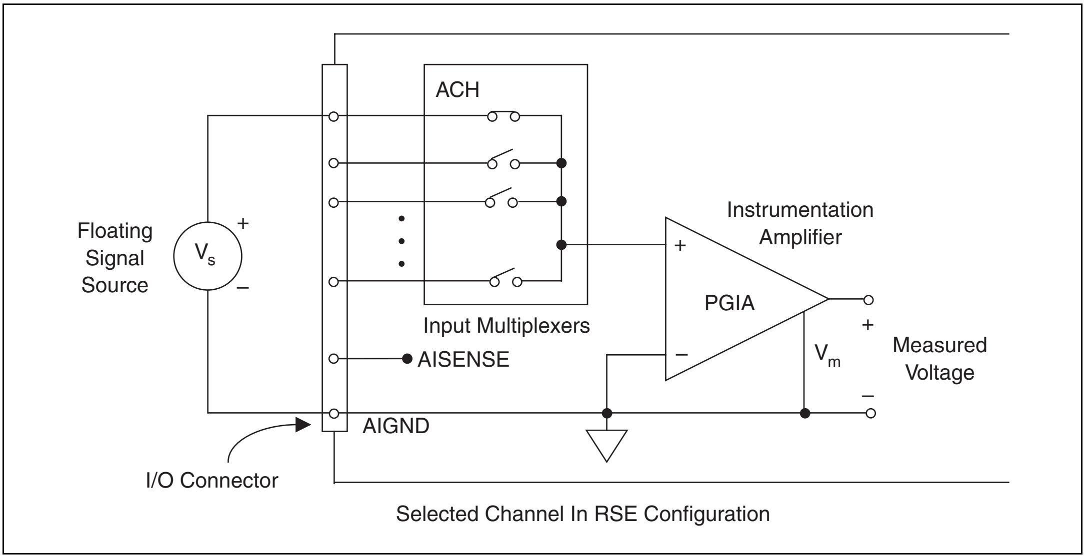


Figure 4-7. Single-Ended Input Connections for Nonreferenced or Floating Signals

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

To measure a grounded signal source with a single-ended configuration, you must configure the device in NRSE input mode. The signal is then connected to the positive input of the PGIA, and the signal local ground reference is connected to the negative input of the PGIA. The ground point of the signal should, therefore, be connected to the AISENSE pin. Any potential difference between the NI 6052E ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA, and this difference is rejected by the amplifier. If the input circuitry of the NI 6052E were referenced to ground, as in the RSE configuration, this difference in ground potentials would appear as an error in the measured voltage.

Figure 4-8 shows how to connect a grounded signal source to a channel on the NI 6052E configured for NRSE input mode.

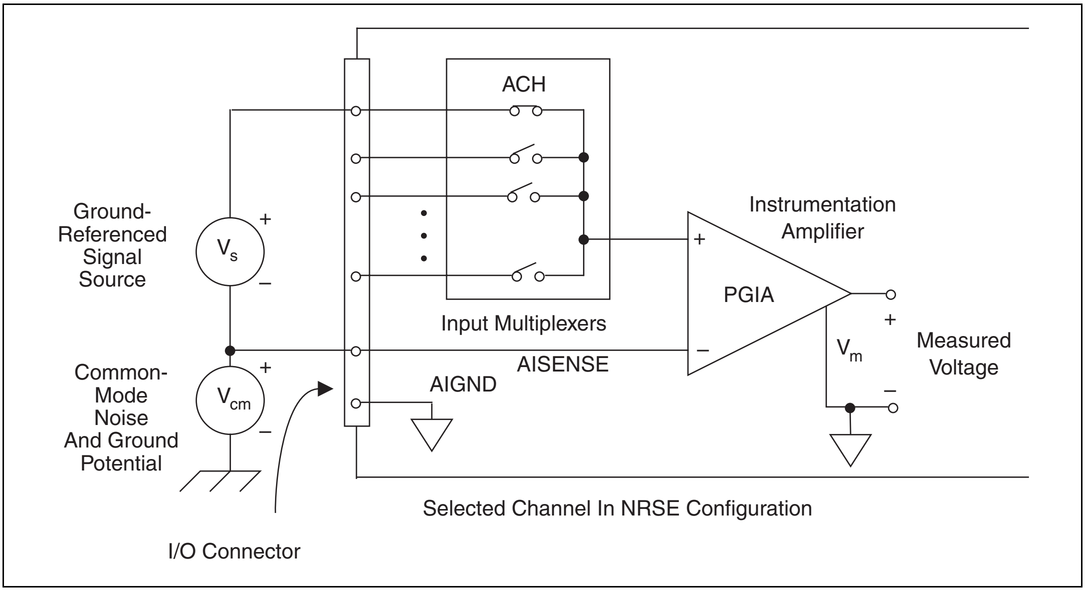


Figure 4-8. Single-Ended Input Connections for Ground-Referenced Signals

Common-Mode Signal Rejection Considerations

Figures 4-6 and 4-8 show connections for signal sources that are already referenced to some ground point with respect to the NI 6052E. In these cases, the PGIA can reject any voltage caused by ground potential differences between the signal source and the device. In addition, with DIFF input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the device. The PGIA can reject common-mode signals as long as $V+_{in}$ and $V-_{in}$ (input signals) are both within ±11 V of AIGND.

Measuring More than Eight Channels with the NI DAQPad-6052E for BNC

The NI DAQPad-6052E for BNC is designed to measure up to eight differential channels using BNC connectors and cabling. To measure more than eight channels, you must use one of the single-ended modes. Up to 16 single-ended channels are available in the single-ended configuration.

To use a single-ended mode, change the source type (FS/GS) switch settings on the device front panel. Figure 4-9 shows the switch locations.

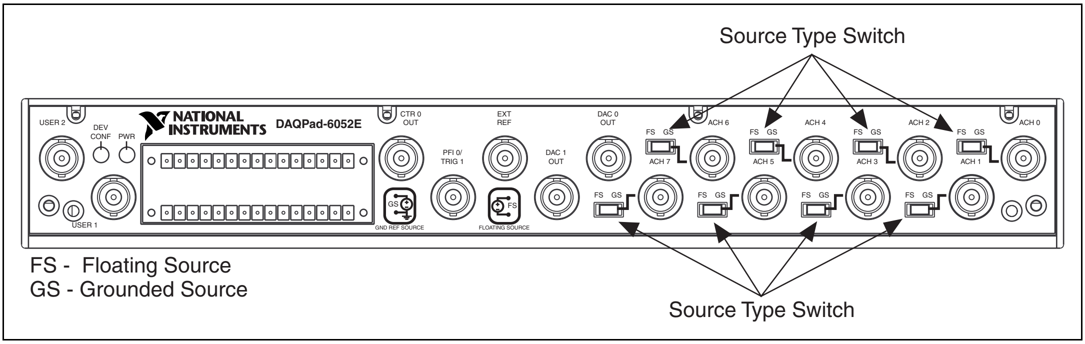


Figure 4-9. Front Panel of the DAQPad-6052E for BNC

For each BNC connector that you use for two channels, set the source type switch to the GS position. This setting disconnects the built-in ground reference resistor from the negative terminal of the BNC connector, allowing it to be used as a single-ended channel, as shown in Figure 4-10. When you set the source type to the GS position and configure the device for single-ended input, each BNC connector provides access to two single-ended channels, ACH(*i*) and ACH(*i*+8). For example, the BNC connector labeled *ACH0* provides access to single-ended channels ACH0 and ACH8, the BNC connector labeled *ACH1* provides access to single-ended channels ACH1 and ACH9, and so on.

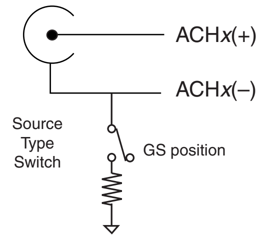


Figure 4-10. BNC Connector Wiring

Connecting Analog Output Signals

The AO signals are DAC0OUT, DAC1OUT, EXTREF, and AOGND.

DAC0OUT and DAC1OUT are the voltage output signals for AO channels 0 and 1, respectively.

EXTREF is the external reference input for both AO channels. You must individually configure each AO channel for external reference selection so that the signal applied at the external reference input is used by that channel. If you do not specify an external reference, the channel uses the internal reference. AO configuration options are explained in the *Analog Output* section in Chapter 3, *Hardware Overview*. The following ranges and ratings apply to the EXTREF input:

- Usable input voltage range: ±11 V peak with respect to AOGND
- Absolute maximum ratings: ±15 V peak with respect to AOGND

AOGND is the ground reference signal for both AO channels and the external reference signal.

Figure 4-11 shows how to make AO connections and the external reference input connection to the device.

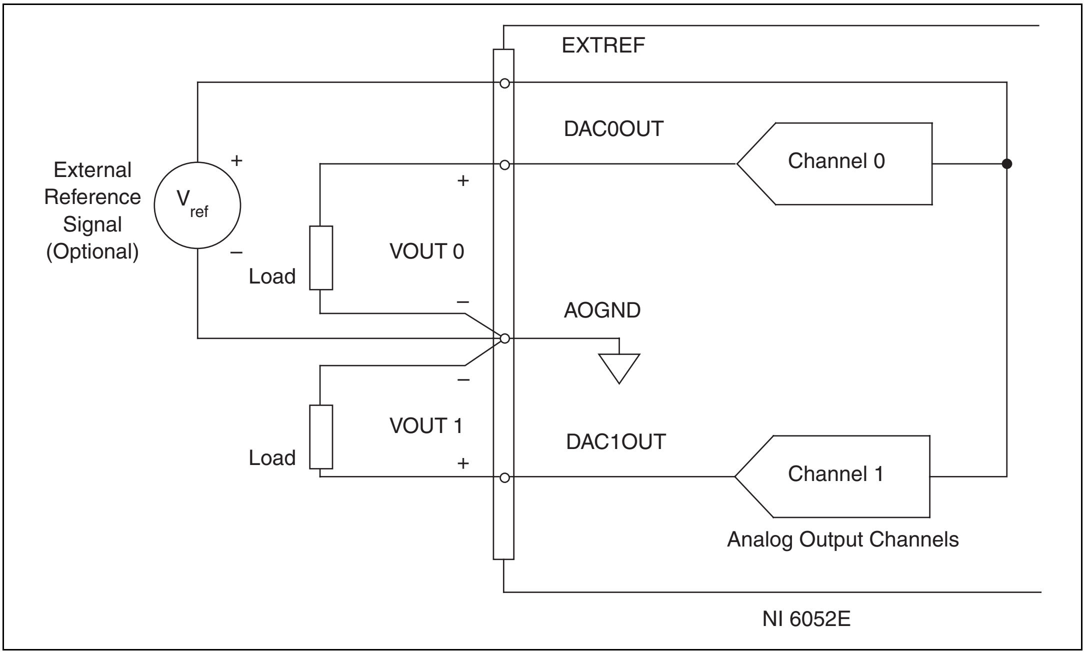


Figure 4-11. Analog Output Connections

The external reference signal can be either a DC or an AC signal. The device multiplies this reference signal by the DAC code (divided by the full-scale DAC code) to generate the output voltage.

Connecting Digital I/O Signals

The DIO signals are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. You can program all lines individually to be inputs or outputs.

Caution Exceeding the maximum input voltage ratings listed in Table 4-2 can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections.

Figure 4-12 shows signal connections for three typical DIO applications. Figure 4-12 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states, such as the state of the switch shown in the figure. Digital output applications include sending TTL signals and driving external devices, such as the LED shown in the figure.

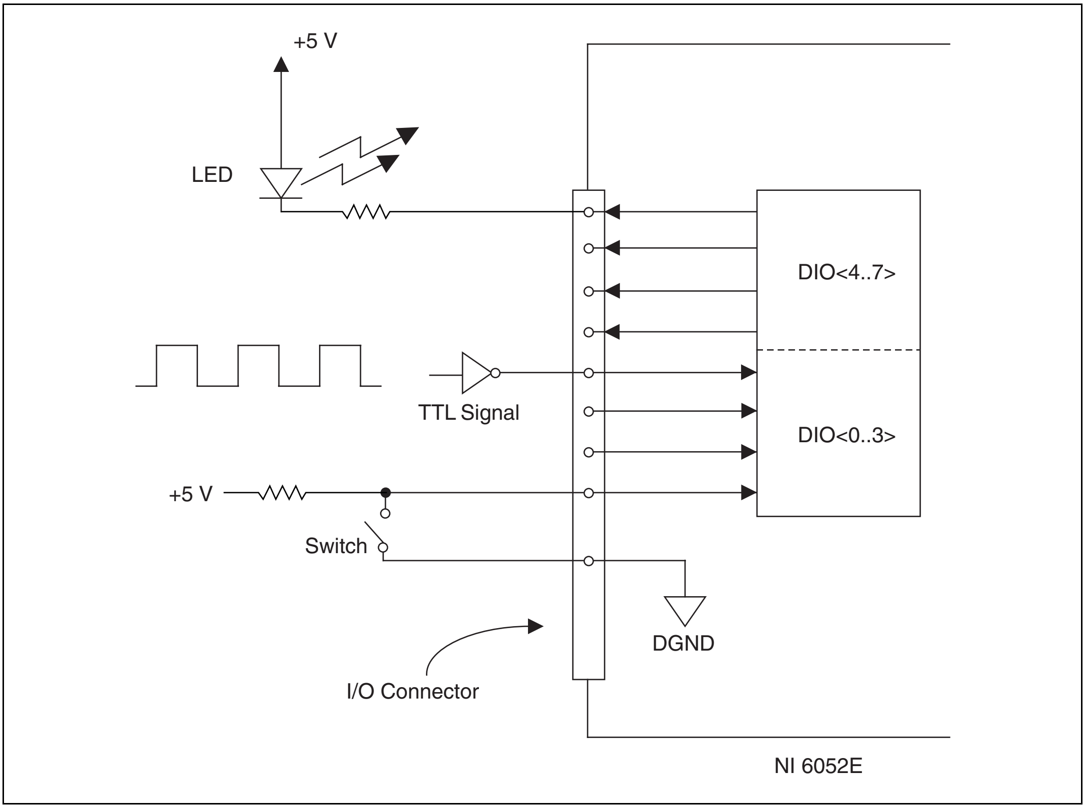


Figure 4-12. Digital I/O Connections

Power Connections

Two pins on the I/0 connector supply +5 V from the computer power supply through a self-resetting fuse. The fuse will reset automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry. The fuse power rating is +4.65 to +5.25 VDC at 1 A.

Caution Under no circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the device or any other device.

Doing so can damage the device and the computer. NI is *not* liable for damage resulting from such a connection.

Connecting Timing Signals

Caution Exceeding the maximum input voltage ratings listed in Tables 4-2 can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections.

All external control over the timing of the device is routed through the ten PFIs labeled *PFI0* through *PFI9*. Refer to the *Programmable Function Input Connections* section for more information on these signals. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many DAQ, waveform generation, and general-purpose timing signals. The NI 6052E has five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any DAQ, waveform generation, and general-purpose timing signals.

Refer to the following sections of this chapter for more information on these signals:

- *Data Acquisition Timing Connections*
- *Waveform Generation Timing Connections*
- *General-Purpose Timing Signal Connections*

All digital timing connections are referenced to DGND. Figure 4-13 shows how to connect an external TRIG1 source and an external CONVERT* source to two NI 6052E PFI pins.

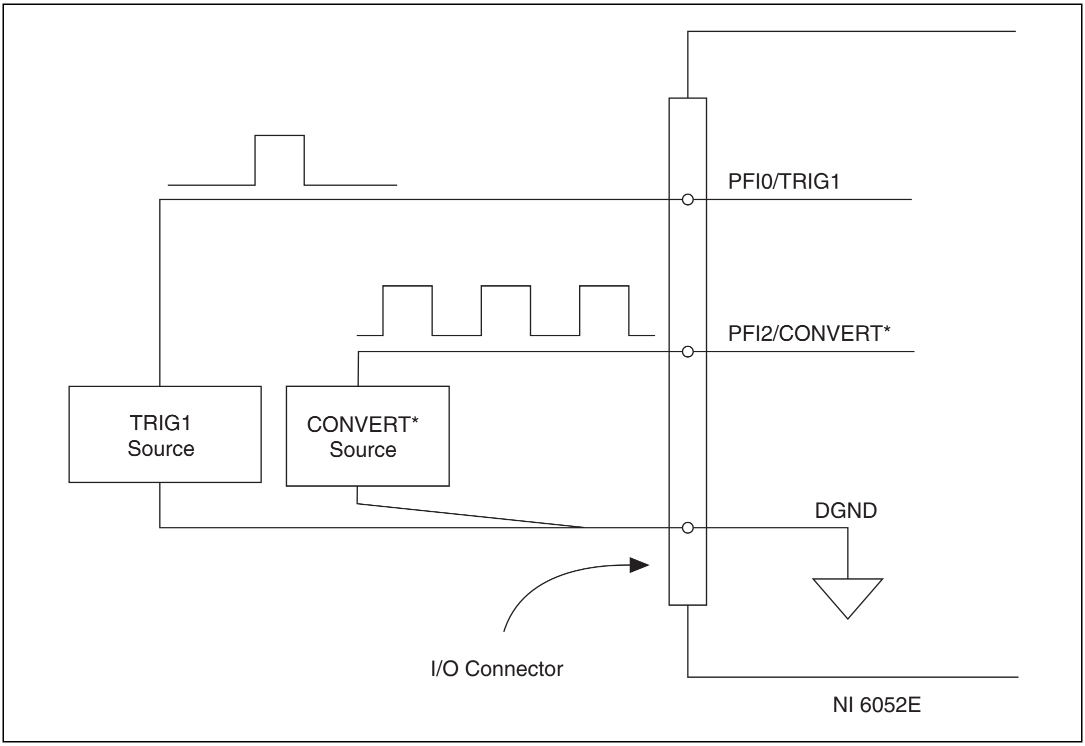


Figure 4-13. Timing I/O Connections

Programmable Function Input Connections

You can externally control 13 internal timing signals from the PFI pins. The source for each of these signals is software configurable from any PFI when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for applications requiring alternative wiring.

You can individually enable each PFI pin to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output to the I/O connector, the application software can turn on the output driver for the PFI2/CONVERT* pin. Be careful not to externally drive a PFI signal when it is configured as an output.

As an input, you can individually configure each PFI signal for edge or level detection and polarity selection. You can use the polarity selection for any timing signal, but the edge or level detection will depend on the particular timing signal being controlled. The detection requirements for each timing signal are listed in the corresponding sections.

In edge-detection mode, the minimum pulse width required is 10 ns. This requirement applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse width requirement in edge-detect mode.

In level-detection mode, there are no pulse width requirements imposed by the PFIs themselves. Limits can be imposed by the particular timing signal being controlled. These requirements are listed in the sections describing the particular signals.

Data Acquisition Timing Connections

The timing signals are TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, SISOURCE, SCANCLK, and EXTSTROBE*.

Posttriggered data acquisition allows you to view data that is acquired after a trigger event is received. Figure 4-14 shows a typical posttriggered sequence.

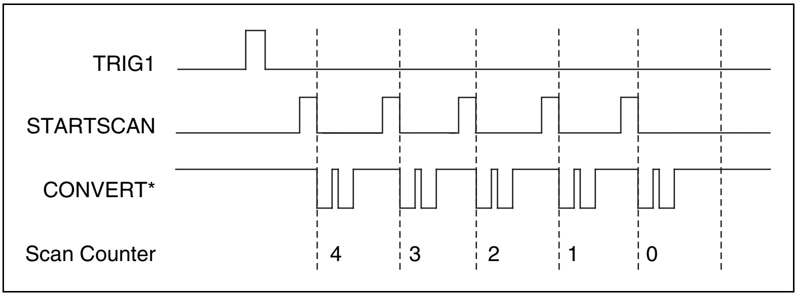


Figure 4-14. Typical Posttriggered Sequence

Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-15 shows a typical pretriggered sequence. The description for each signal shown in these figures is included later in this chapter.

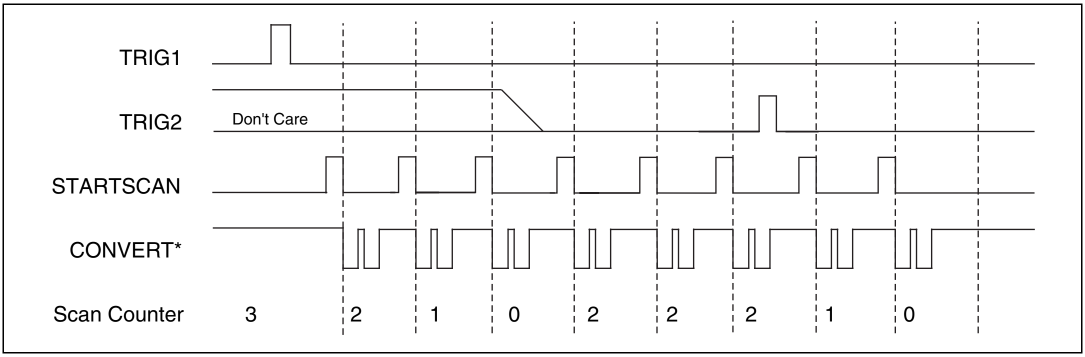


Figure 4-15. Typical Pretriggered Sequence

TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

As an input, TRIG1 is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of TRIG1 starts the sequence for both posttriggered and pretriggered acquisitions. Refer to Figures 4-14 and 4-15 for the relationship of TRIG1 to the sequence. Refer to Chapter 3, *Hardware Overview*, for more information on analog triggering.

As an output, TRIG1 reflects the action that initiates a sequence, even if the acquisition is externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-16 and 4-17 show the input and output timing requirements for TRIG1.

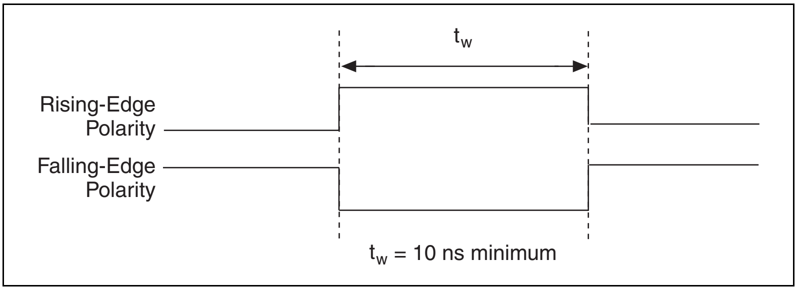


Figure 4-16. TRIG1 Input Signal Timing

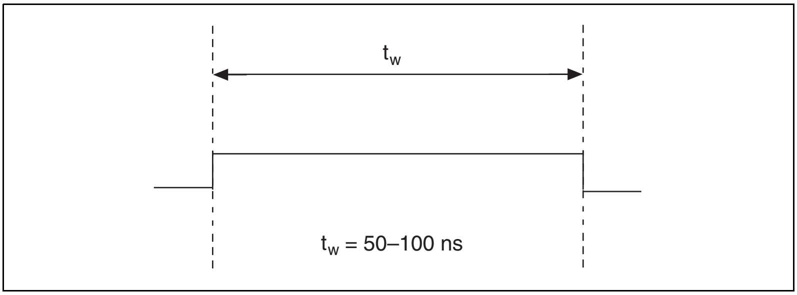


Figure 4-17. TRIG1 Output Signal Timing

The device also uses TRIG1 to initiate pretriggered operations. In pretriggered applications, TRIG1 is generated by a software trigger unless a PFI pin is selected as the source of TRIG1. Refer to the *TRIG2 Signal* section of this chapter for a complete description of the use of TRIG1 and TRIG2 in a pretriggered operation.

TRIG2 Signal

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin. Refer to Figure 4-15 for the relationship of TRIG2 to the sequence.

As an input, TRIG2 is configured in edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of TRIG2 initiates the posttriggered phase of a pretriggered sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter indicates the minimum number of scans before TRIG2 can be recognized. After the scan counter decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device ignores TRIG2 if it is asserted prior to the scan counter decrementing to zero. After the selected edge of TRIG2 is received, the device acquires a fixed number of scans and the acquisition stops. In pretriggered mode, the device acquires data both before and after receiving TRIG2.

As an output, TRIG2 reflects the posttrigger in a pretriggered sequence, even if the acquisition is externally triggered by another PFI. TRIG2 is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-18 and 4-19 show the input and output timing requirements for TRIG2.

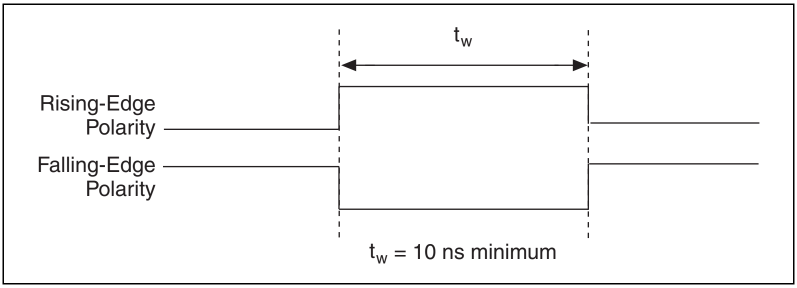


Figure 4-18. TRIG2 Input Signal Timing

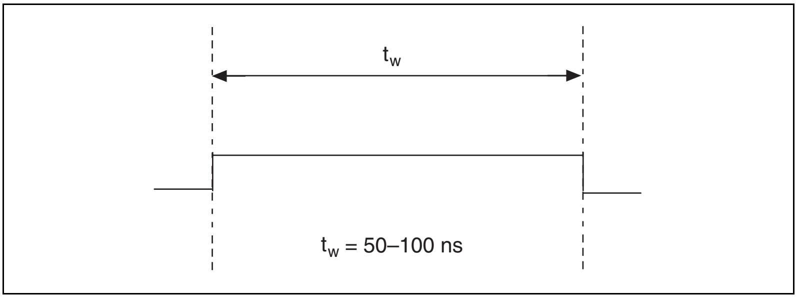


Figure 4-19. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can externally input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin. Refer to Figures 4-14 and 4-15 for the relationship of STARTSCAN to the sequence.

As an input, STARTSCAN is configured in edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of STARTSCAN initiates a scan. The sample interval counter starts if you select an internally triggered CONVERT*.

As an output, STARTSCAN reflects the actual start pulse that initiates a scan, even if the starts are being externally triggered by another PFI. You have two output options. The first option is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan. The second option is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN will be deasserted t_{off} after the last conversion in the scan is initiated. This output is set to high-impedance at startup.

Figures 4-20 and 4-21 show the input and output timing requirements for STARTSCAN.

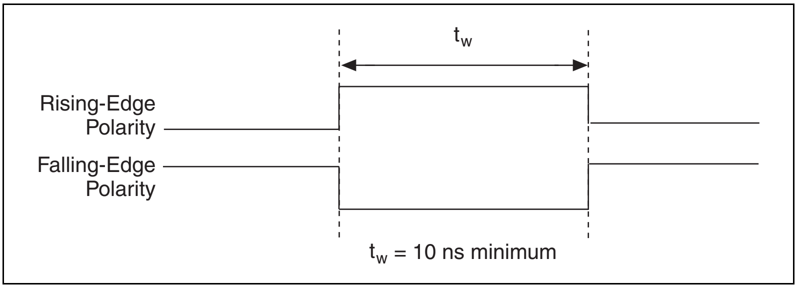


Figure 4-20. STARTSCAN Input Signal Timing

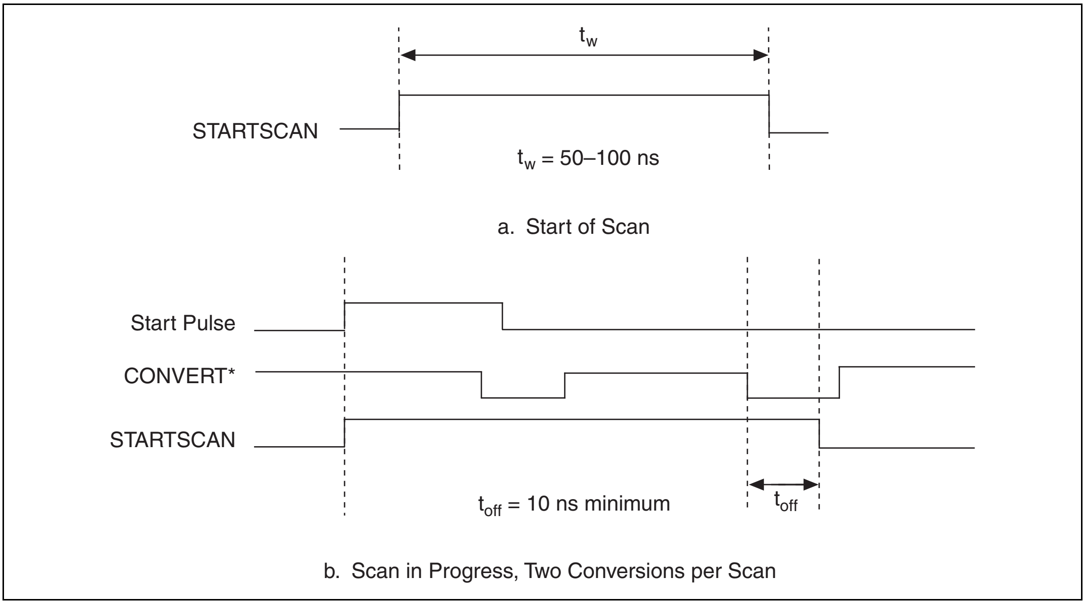


Figure 4-21. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the device generates STARTSCAN. If you use internally generated conversions, the first CONVERT* appears when the onboard sample interval counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN generates a conversion. Separate the STARTSCAN pulses by at least one scan period.

A counter on the device internally generates STARTSCAN unless you select some external source. The TRIG1 signal starts this counter, and the application software or the sample counter stops it.

Scans generated by either an internal or external STARTSCAN are inhibited unless they occur within a sequence. Scans occurring within a sequence can be gated by either the hardware AIGATE signal or the software command register gate.

CONVERT* Signal

Any PFI pin can externally input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-14 and 4-15 for the relationship of CONVERT* to the sequence.

As an input, CONVERT* is configured in edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of CONVERT* initiates an A/D conversion.

As an output, CONVERT* reflects the actual convert pulse that is connected to the ADC, even if the conversions are being externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-22 and 4-23 show the input and output timing requirements for CONVERT*.

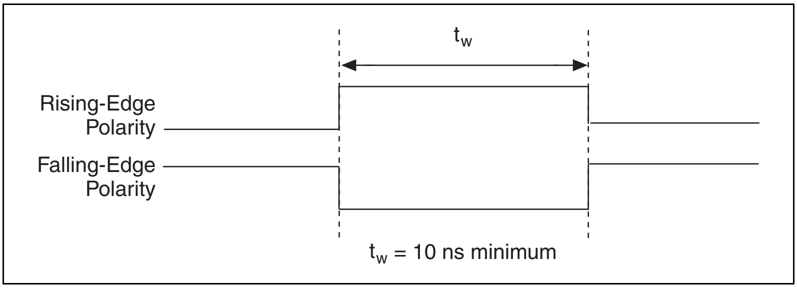


Figure 4-22. CONVERT* Input Signal Timing

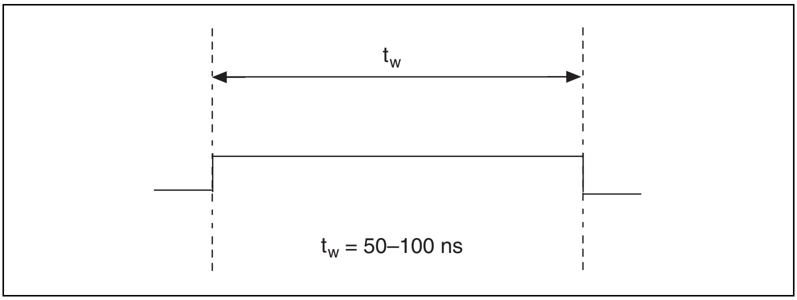


Figure 4-23. CONVERT* Output Signal Timing

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. Separate the CONVERT* pulses by at least one conversion period.

The sample interval counter on the NI 6052E generates CONVERT* unless you select an external source. The STARTSCAN signal starts the counter, which continues to count down and reload itself until the scan is finished. It then reloads itself in preparation for the next STARTSCAN pulse.

A/D conversions generated by an internal or external CONVERT* signal are inhibited unless they occur within a sequence. Scans occurring within a sequence can be gated by either the hardware AIGATE signal or the software command register gate.

AIGATE Signal

Any PFI pin can externally input the AIGATE signal, which is not available as an output on the I/O connector. AIGATE can mask off scans in a sequence. You can configure the PFI pin you select as the source for AIGATE in either the level-detection or edge-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

In the level-detection mode with AIGATE is active, the STARTSCAN signal is masked off and no scans can occur. In the edge-detection mode, the first active edge disables STARTSCAN, and the second active edge enables STARTSCAN.

AIGATE can neither stop a scan in progress nor continue a previously gated-off scan. In other words, once a scan has started, AIGATE does not gate off conversions until the beginning of the next scan. Conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval counter uses SISOURCE as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for SISOURCE in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency.

Either the 20 MHz or 100 kHz internal timebase generates SISOURCE unless you select an external source. Figure 4-24 shows the timing requirements for SISOURCE.

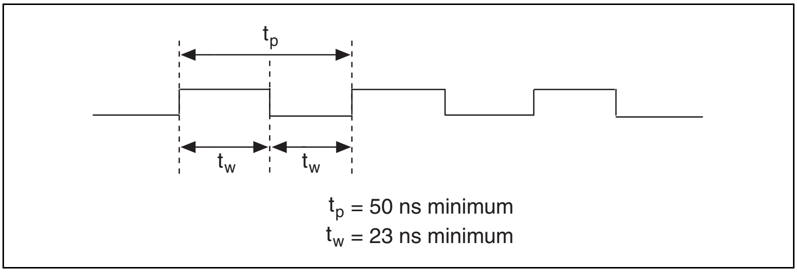


Figure 4-24. SISOURCE Signal Timing

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software configurable, but the polarity is typically configured so that a low-to-high leading edge can clock external analog input multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled. Figure 4-25 shows the timing for SCANCLK.

Note The polarity of SCANCLK is not software-selectable when programmed using NI-DAQ. It is a positive polarity pulse.

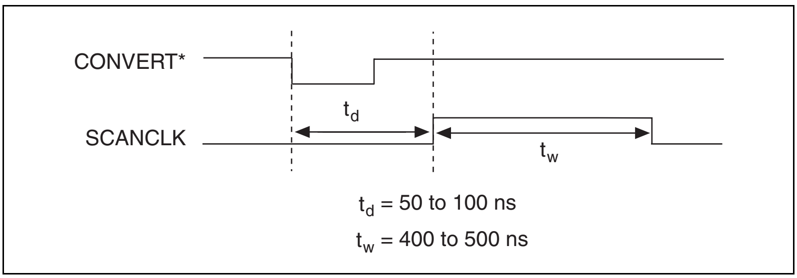


Figure 4-25. SCANCLK Signal Timing

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, the application software controls the level of EXTSTROBE*. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode. Figure 4-26 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

Note EXTSTROBE cannot be controlled using NI-DAQ.

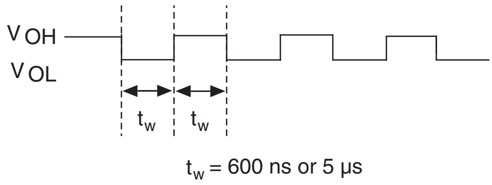


Figure 4-26. EXTSTROBE* Signal Timing

Waveform Generation Timing Connections

The analog group defined for the device is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, WFTRIG is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of WFTRIG starts the waveform generation for the DACs. If you select internally generated UPDATE*, the update interval (UI) counter starts.

As an output, WFTRIG reflects the trigger that initiates waveform generation, even if the waveform generation is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to high-impedance at startup.

Figures 4-27 and 4-28 show the input and output timing requirements for WFTRIG.

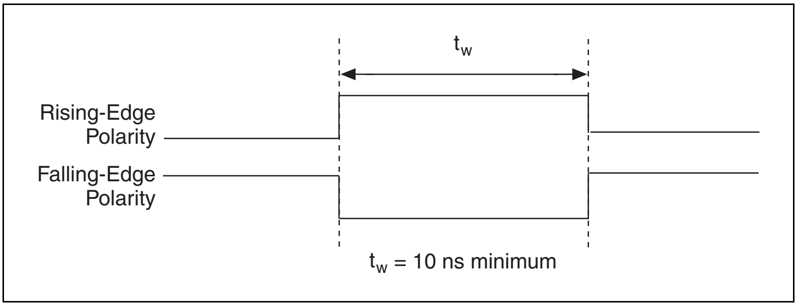


Figure 4-27. WFTRIG Input Signal Timing

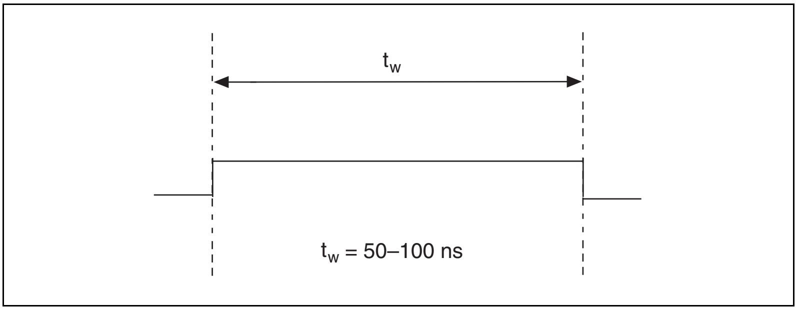


Figure 4-28. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, UPDATE* is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of UPDATE* updates the outputs of the DACs. To use UPDATE*, you must set the DACs to posted-update mode.

As an output, UPDATE* reflects the actual update pulse connected to the DACs, even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 300 to 350 ns. This output is set to high-impedance at startup.

Figures 4-29 and 4-30 show the input and output timing requirements for UPDATE*.

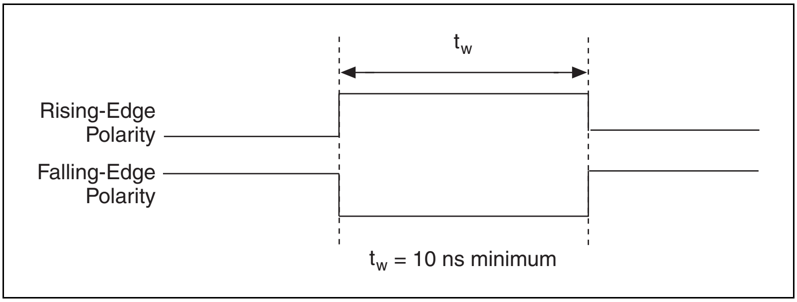


Figure 4-29. UPDATE* Input Signal Timing

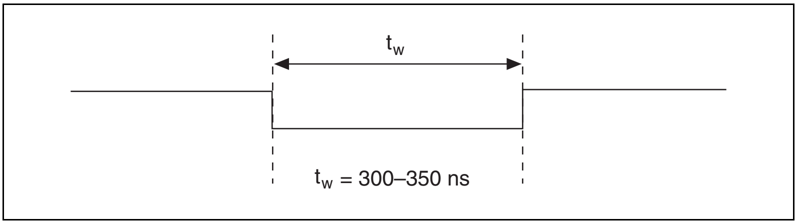


Figure 4-30. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time so that new data can be written to the DAC latches.

The NI 6052E UI counter normally generates UPDATE* unless you select an external source. The UI counter is started by the WFTRIG signal and can be stopped by the application software or the internal Buffer Counter, which is a counter for FIFO memory.

D/A conversions generated by an internal or external UPDATE* signal do not occur when gated by the software command register gate.

When using an external UPDATE* signal, supply at least one more external update pulse than the number of points you want to generate. Otherwise, the device does not indicate that the waveform generation is complete.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector.

The UI counter uses UISOURCE as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for UISOURCE in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency.

Either the 20 MHz or 100 kHz internal timebase normally generates UISOURCE unless you select an external source.

Figure 4-31 shows the timing requirements for UISOURCE.

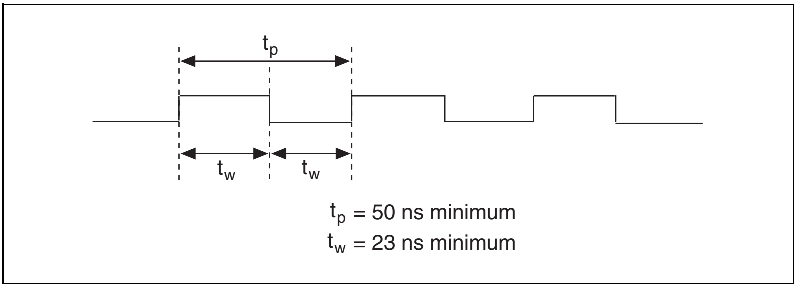


Figure 4-31. UISOURCE Signal Timing

General-Purpose Timing Signal Connections

The general-purpose timing signals are as follows:

- GPCTR0_SOURCE
- GPCTR0_GATE
- GPCTR0_OUT
- GPCTR0_UP_DOWN
- GPCTR1_SOURCE
- GPCTR1_GATE
- GPCTR1_OUT
- GPCTR1_UP_DOWN
- FREQ_OUT

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, the GPCTR0_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR0_SOURCE reflects the actual clock connected to general-purpose counter 0, even if another PFI is externally inputting the source clock. This output is set to high-impedance at startup.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency.

The 20 MHz or 100 kHz timebase normally generates GPCTR0_SOURCE unless you select some external source.

Figure 4-32 shows the timing requirements for GPCTR0_SOURCE.

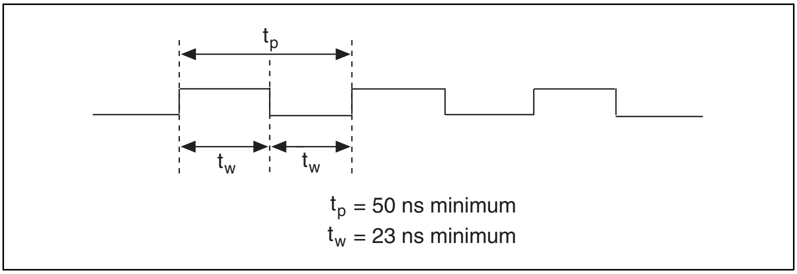


Figure 4-32. GPCTR0_SOURCE Signal Timing

GPCTR0_GATE Signal

Any PFI pin can externally input GPCTR0_GATE, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, GPCTR0_GATE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in different applications to perform actions such as starting and stopping the counter, generating interrupts, and saving the counter contents.

As an output, GPCTR0_GATE reflects the actual gate signal connected to general-purpose counter 0, even if the gate is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-33 shows the timing requirements for GPCTR0_GATE.

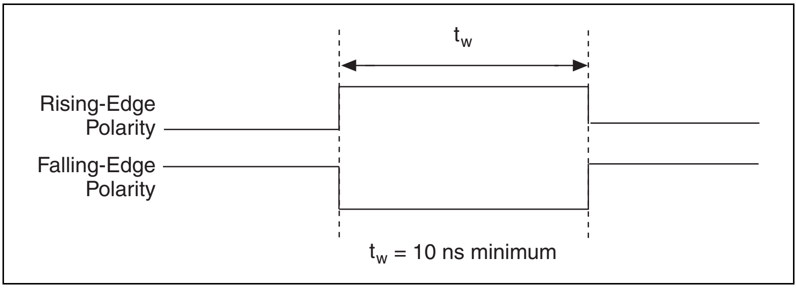


Figure 4-33. GPCTR0_GATE Signal Timing

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. GPCTR0_OUT reflects the terminal count (TC) of general-purpose counter 0. You have two software-configurable output options—pulse on TC and toggle output polarity on TC. The output polarity is software configurable for both options. This output is set to high-impedance at startup.

Figure 4-34 shows the timing of GPCTR0_OUT.

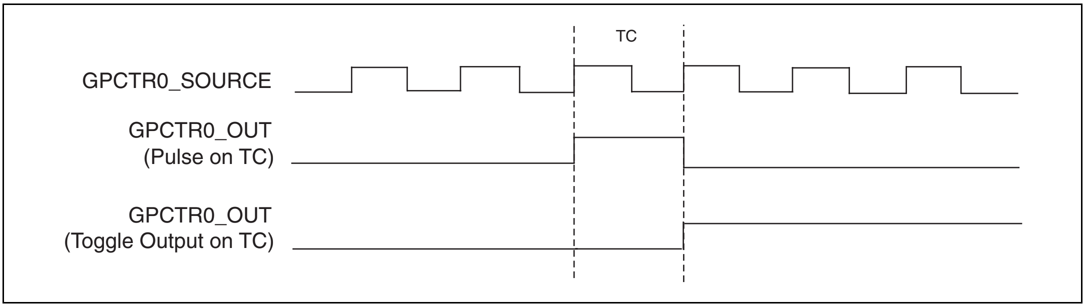


Figure 4-34. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 counts down when this pin is at a logic low, and it counts up when it is at a logic high. You can disable this input so that the application software controls the up-down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, GPCTR1_SOURCE is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1, even if the source clock is being externally generated by another PFI. This output is set to high-impedance at startup.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency.

The 20 MHz or 100 kHz timebase normally generates GPCTR1_SOURCE unless you select some external source.

Figure 4-35 shows the timing requirements for GPCTR1_SOURCE.

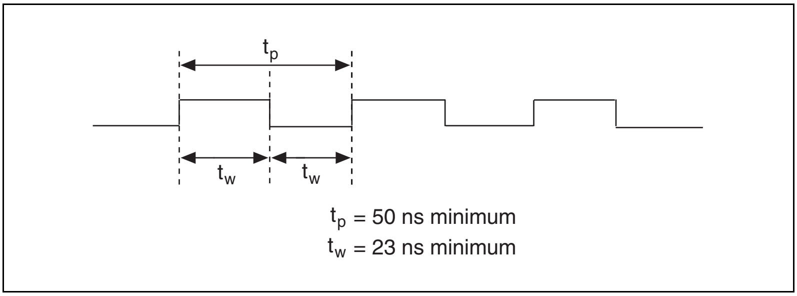


Figure 4-35. GPCTR1_SOURCE Signal Timing

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, GPCTR1_GATE is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of applications to perform actions such as starting and stopping the counter, generating interrupts, and saving the counter contents.

As an output, GPCTR1_GATE monitors the actual gate signal connected to general-purpose counter 1, even if the gate is being externally generated by another PFI. This output is set to high-impedance at startup.

Figure 4-36 shows the timing requirements for GPCTR1_GATE.

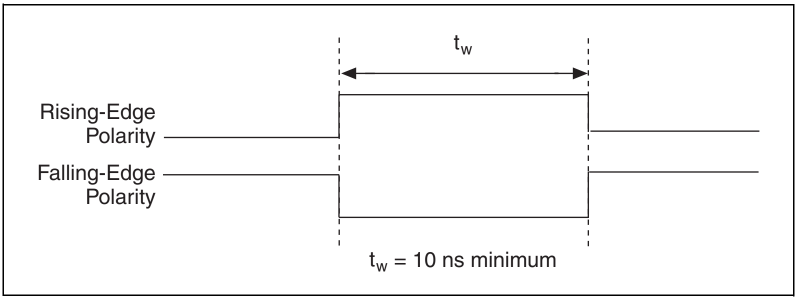


Figure 4-36. GPCTR1_GATE Signal Timing

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC device general-purpose counter 1. You have two software-configurable output options—pulse on TC and toggle output polarity on TC. The output polarity is software configurable for both options. This output is set to high-impedance at startup.

Figure 4-37 shows the timing requirements for GPCTR1_OUT.

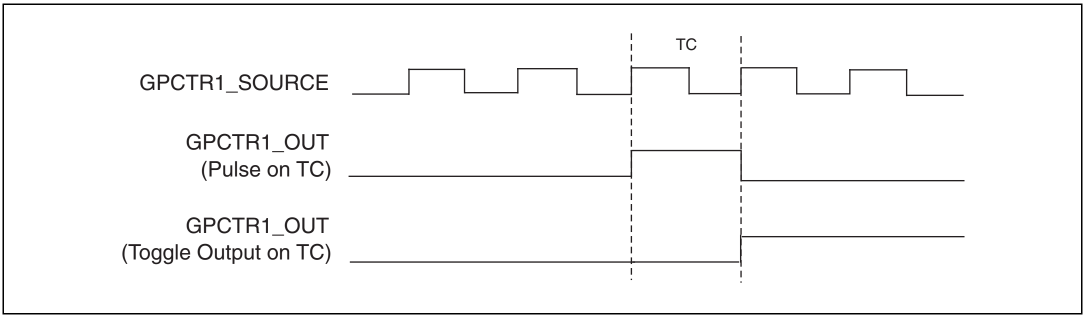
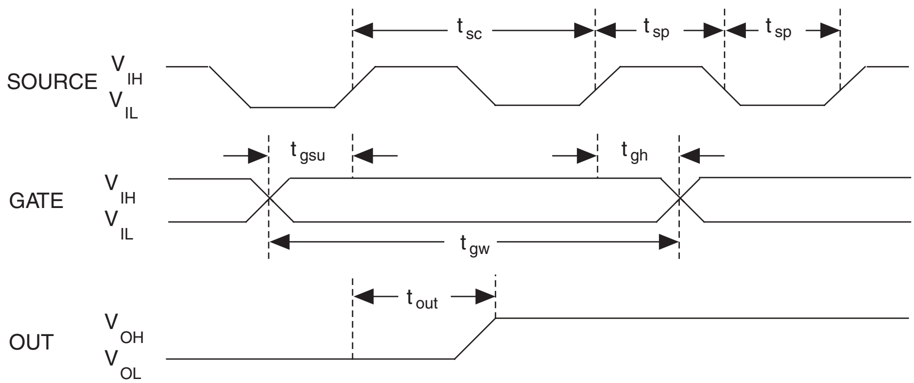


Figure 4-37. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that the application software controls the up-down functionality and leave the DIO7 pin free for general use.

Figure 4-38 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of the device.



Source Clock Period	t_{sc}	50 ns minimum
Source Pulse Width	t_{sp}	23 ns minimum
Gate Setup Time	t_{gsu}	10 ns minimum
Gate Hold Time	t_{gh}	0 ns minimum
Gate Pulse Width	t_{gw}	10 ns minimum
Output Delay Time	t_{out}	80 ns maximum

Figure 4-38. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-38 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. If the counter was programmed to count falling edges, the source signal would be inverted and referenced to the falling edge of the source signal in Figure 4-38.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on the device. Figure 4-38 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-38. The gate signal is not required to be held after the active edge of the source signal.

If you use an internal timebase clock, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the NI 6052E. Figure 4-38 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal, generated by the NI 6052E frequency generator, is available only as an output on the FREQ_OUT pin. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software configurable from the internal 10 MHz and 100 kHz timebases. The output polarity is software configurable. This output is set to high-impedance at startup.

Field Wiring Considerations

Environmental noise can seriously affect the accuracy of measurements if you do not take proper care when running signal wires between signal sources and the device.

The following recommendations mainly apply to analog input signal routing to the device, although they also apply to signal routing in general:

- Use differential analog input connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect analog input signals to the device. With this type of wire, the signals attached to the CH+ and CH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a PCI DAQ system is the

video monitor. Separate the monitor from the analog signals as far as possible.

The following recommendations apply for all signal connections to the device:

- Separate NI 6052E signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the NI 6052E signal lines if they run in parallel paths at a close distance.

  To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel or run the lines at right angles to each other.
- Do *not* run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

Refer to the NI Developer Zone tutorial, *Field Wiring and Noise Consideration for Analog Signals,* available at `ni.com/zone`.

5

Calibration

This chapter discusses the calibration procedure for the device.

Calibration is the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the NI 6052E, these adjustments take the form of writing values to onboard calibration DACs (CalDACs). NI-DAQ includes calibration functions for performing all of the steps in the calibration process.

Some form of device calibration is required for almost all applications. If you do not calibrate the device, the signals and measurements could have very large offset, gain, and linearity errors.

Three available levels of calibration are described in this chapter. The first level, loading calibration constants, is the fastest, easiest, and least accurate. The last level, external calibration, is the slowest, most difficult, and most accurate. Choose a level according to the demands of your application.

Loading Calibration Constants

Before shipment, the device is factory-calibrated at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the device is unpowered. Loading calibration constants is the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ determines when this is necessary and automatically loads calibration constants. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM there is a user-modifiable calibration area in addition to the permanent factory calibration area. You can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

This method of calibration is not very accurate because it does not take into account the fact that the device measurement and output voltage errors can vary with time and temperature. You should self-calibrate when the device is installed in the environment in which it will be used.

Self-Calibration

The device can measure and correct for almost all of its calibration-related errors without any external signal connections. NI software provides a self-calibration method, which generally takes less than a minute and is the preferred method of ensuring accuracy in your application. Initiate self-calibration to minimize the effects of any offset, gain, and linearity drifts, particularly those due to the device not being fully warmed up.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration is sufficient.

External Calibration

The device has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using the device at an extreme temperature or if the onboard reference has not been measured for a year or more, you can externally calibrate the device.

External calibration is the process of calibrating the device with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process, and the results can be saved in the EEPROM, so you will not need to perform an external calibration very often. You can externally calibrate the device by calling the NI-DAQ calibration function.

To externally calibrate the device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself. For example, to calibrate a 16-bit device, the external reference should be at least ±0.001% (±10 ppm) accurate.

Other Considerations

The CalDACs adjust the gain error of each AO channel by adjusting the value of the reference voltage supplied to that channel. This calibration mechanism is designed to work only with the internal 10 V reference. Thus, in general, it is not possible to calibrate the AO gain error when using an external reference. In this case, account for the nominal gain error of the AO channel either in software or with external hardware. Refer to Appendix A, *Specifications*, for information on AO gain error.

Gain error and offset error are temperature dependent. Turn on the NI 6052E for the recommended warmup time in a stable temperature environment before calibrating the device. Refer to Appendix A, *Specifications*, to determine the warmup time. The device should be calibrated at the temperature at which it will operate.

For more information on calibrating the device, refer to `ni.com/calibration`.

A Specifications

This appendix lists the specifications of the NI 6052E. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels

PCI/PXI-6052E,
DAQPad-6052E .... 16 single-ended or 8 differential (software-selectable)

Type of ADC... Successive approximation

Resolution .... 16 bits, 1 in 65,536

Max sampling rate................................. 333 kS/s guaranteed

Input signal ranges

Device Gain (Software-Selectable)	Device Range (Software-Selectable)	
	Bipolar	Unipolar
0.5	±10 V	—
1	±5 V	0 to 10 V
2	±2.5 V	0 to 5 V
5	±1 V	0 to 2 V
10	±500 mV	0 to 1 V
20	±250 mV	0 to 500 mV
50	±100 mV	0 to 200 mV
100	±50 mV	0 to 100 mV

NI 6052E Accuracy Information

Nominal Range (V)		Absolute Accuracy							Relative Accuracy	
		% of Reading			Offset	Noise + Quantization (µV)		Temp Drift	Resolution (µV)	
Positive FS	Negative FS	24 Hours	90 Days	1 Year	(µV)	Single Pt.	Avg.	(%/°C)	Single Pt.	Avg.
10	–10	0.0304	0.0312	0.0321	1067	981	87.0	0.0006	1145	115
5	–5	0.0054	0.0062	0.0071	536	491	43.5	0.0001	573	57.3
2.5	–2.5	0.0304	0.0312	0.0321	271	245	21.7	0.0006	286	28.6
1	–1	0.0304	0.0312	0.0321	111	98.1	8.7	0.0006	115	11.5
0.5	–0.5	0.0304	0.0312	0.0321	58.1	56.2	5.0	0.0006	66.3	6.6
0.25	–0.25	0.0304	0.0312	0.0321	31.6	32.8	3.0	0.0006	39.2	3.9
0.1	–0.1	0.0304	0.0312	0.0321	15.6	22.4	2.1	0.0006	27.7	2.8
0.05	–0.05	0.0304	0.0312	0.0321	10.3	19.9	1.9	0.0006	25.3	2.5
10	0	0.0054	0.0062	0.0071	536	491	43.5	0.0001	573	57.3
5	0	0.0304	0.0312	0.0321	271	245	21.7	0.0006	286	28.6
2	0	0.0304	0.0312	0.0321	111	98.1	8.7	0.0006	115	11.5
1	0	0.0304	0.0312	0.0321	58.1	56.2	5.0	0.0006	66.3	6.6
0.5	0	0.0304	0.0312	0.0321	31.6	39.8	3.0	0.0006	48.2	3.9
0.2	0	0.0304	0.0312	0.0321	15.6	22.4	2.1	0.0006	27.7	2.8
0.1	0	0.0304	0.0312	0.0321	10.3	19.9	1.9	0.0006	25.3	2.5

Note: Accuracies are valid for measurements following an internal E Series Calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings.

Measurement accuracies are listed for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of external or factory calibration temperature.

Input coupling..DC

Max working voltage
(signal + common-mode)........................Each input should remain within ±11 V of ground

Overvoltage protection ....±25 V powered on, ±15 V powered off

Inputs protected

NI PCI/PXI-6052E,
NI DAQPad-6052E ....ACH<0..15>, AISENSE

FIFO buffer size .... 512 samples

Data transfers .... DMA, interrupts, programmed I/O

DMA modes .... Scatter-gather

Configuration memory size.................... 512 words

Transfer Characteristics

Relative accuracy .... ±1.5 LSB typ, ±3.0 LSB max

DNL .... ±0.5 LSB typ, ±1.0 LSB max

No missing codes .... 16 bits, guaranteed

Offset error

- Pregain error after calibration .... ±1.0 μV max
- Pregain error before calibration ...... ±2.6 mV max
- Postgain error after calibration .... ±76 μV
- Postgain error before calibration..... ±82 mV

Gain error (relative to calibration reference)

- After calibration (gain = 1) .... ±30.5 ppm of reading max
- Before calibration .... ±22,000 ppm of reading max

Gain ≠ 1 with gain error
adjusted to 0 at gain = 1 .... ±200 ppm of reading max

Amplifier Characteristics

Input impedance

- Normal powered on .... 100 GΩ in parallel with 100 pF
- Powered off.................................... 820 Ω min
- Overload.. 820 Ω min

Input bias current .... ±200 pA

Input offset current................................ ±100 pA

CMRR, DC to 60 Hz

- Gain = 0.5 .... 92 dB

Gain = 1 ....97 dB
Gain = 2 ....101 dB
Gain = 5 ....104 dB
Gain ≥ 10 ....105 dB

Dynamic Characteristics

Bandwidth

Small signal (–3 dB)........................480 kHz
Large signal (1% THD)...................500 kHz

Dynamic range.......................................87 dB, ±10 V input, gain 0.5 to 5
83 dB, gain 10

Settling time for full-scale step

Full-Scale Step Accuracy	Settling Time
±16 LSB	3 µs typical
±4 LSB	4 µs max
±2 LSB	5 µs max, gain 0.5 to 10 8 µs max, gain 20 to 50 10 µs max, gain 100
±1 LSB	10 µs max, gain 0.5 to 5 15 µs max, gain 10 to 100
±1/2 LSB	20 µs typical

System noise (including quantization noise)

Gain	Noise
0.5 to 5	0.95 LSBrms
10	1.1 LSBrms
20	1.3 LSBrms
50	2.3 LSBrms
100	4.2 LSBrms

Crosstalk (DC to 100 kHz)

Adjacent channels .... –75 dB

All other channels .... –90 dB

Stability

Recommended warm-up time

NI PCI/PXI-6052E,
NI DAQPad-6052E......................... 15 minutes

Offset temperature coefficient

Pregain .... ±4 μV/°C

Bipolar postgain............................. ±120 μV/°C

Unipolar postgain............................ ±30 μV/°C

Gain temperature coefficient.................. ±17 ppm/°C

Onboard calibration reference

Level .... 5.000 V (±1.0 mV) (over full operating temperature, actual value stored in EEPROM)

Temperature coefficient................. ±0.6 ppm/°C max

Long-term stability .... ±6 ppm/$\sqrt{1{,}000\text{h}}$

Analog Output

Output Characteristics

Number of channels .... 2 voltage

Resolution .... 16 bits, 1 in 65,536

Max update rate ....333 kS/s

Type of DAC ....Double buffered, multiplying

FIFO buffer size....................................2,048 samples

Data transfers...DMA, interrupts, programmed I/O

DMA modes ....Scatter-gather

NI PCI/PXI-6052E and NI DAQPad-6052E Accuracy Information

Nominal Range (V)		Absolute Accuracy				
		% of Reading			Offset	Temp Drift
Positive FS	Negative FS	24 Hrs	90 Days	1 Year	(µV)	(%/°C)
10	–10	0.0044%	0.0052%	0.0061%	±798 µV	0.0001%
10	0	0.0044%	0.0052%	0.0061%	±569 µV	0.0001%
Absolute Accuracy = (% of Reading × Voltage) + Offset + (Temp Drift × Voltage)						
Note: Temp drift applies only if ambient is greater than ±10 °C of previous external calibration.						

Transfer Characteristics

Relative accuracy (INL)

- After calibration..............................±0.35 LSB typ, ±1.0 LSB max
- Before calibration ....±4 LSB max

DNL

- After calibration..............................±0.5 LSB typ, ±1.0 LSB max
- Before calibration ....±3 LSB max

Monotonicity ....16 bits, guaranteed after calibration

Offset error

- After calibration..............................±305 µV max
- Before calibration ....±17 mV max

Gain error (relative to internal reference)

- After calibration .... ±30.5 ppm of output max
- Before calibration .... ±9,000 ppm of output max

Gain error
(relative to external reference) .... +0% to +0.5% of output max, not adjustable

Voltage Output

Ranges .... ±10 V, 0 to 10 V, ± EXTREF, 0 to EXTREF (software-selectable)

Output coupling..................................... DC

Output impedance .... 0.1 Ω max

Current drive .... ±5 mA max

Protection .... Short-circuit to ground

Power-on state....................................... ±0.020 V max

External reference input

- Range .... ±11 V
- Overvoltage protection .... ±25 V powered on, ±15 V powered off
- Input impedance.............................. 10 kΩ
- Bandwidth (–3 dB).......................... 3 kHz
- Slew rate .... 0.3 V/µs

Dynamic Characteristics

Settling time for full-scale step .... 3.5 µs to ±1.0 LSB accuracy

Settling time for half-scale step .... 3.0 µs to ±1.0 LSB accuracy

Slew rate.. 15 V/µs

Noise .... 60 µVrms, DC to 1 MHz

Glitch energy (at midscale transition)

Magnitude..10 mV

Duration...1 µs

Stability

Offset temperature coefficient ....±35 µV/°C

Gain temperature coefficient

Internal reference.............................±6.5 ppm/°C

External reference............................±5 ppm/°C

Onboard calibration reference

Level ....5.000 V (±1.0 mV) (over full operating temperature, actual value stored in EEPROM)

Temperature coefficient...................±0.6 ppm/°C max

Long-term stability ....±6 ppm/ $\sqrt{1{,}000h}$

Digital I/O

Number of channels................................8 input/output

Compatibility ....TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state ....Input (High-Z)

Data transfers ....Programmed I/O

Timing I/O

Number of channels .... 2 up/down counter/timers, 1 frequency scaler

Resolution

- Counter/timers .... 24 bits
- Frequency scalers............................ 4 bits

Compatibility .... TTL/CMOS

Base clocks available

- Counter/timers .... 20 MHz, 100 kHz
- Frequency scalers............................ 10 MHz, 100 kHz

Base clock accuracy .... ±0.01%

Max source frequency .... 20 MHz

Min source pulse duration...................... 10 ns in edge-detect mode

Min gate pulse duration.......................... 10 ns in edge-detect mode

Data transfers .... DMA, interrupts, programmed I/O

DMA modes .... Scatter-gather

Triggers

Analog Trigger

Source

- NI PCI/PXI-6052E, NI DAQPad-6052E......................... ACH<0..15>, PFI0/TRIG1

Level.. ± full-scale, internal; ±10 V, external

Slope.. Positive or negative (software selectable)

Resolution .... 12 bits, 1 in 4,096

Hysteresis .... Programmable

Bandwidth (–3 dB) ....700 kHz internal, 700 kHz external

External input (PFI0/TRIG1)

- Impedance.......................................10 kΩ
- Coupling ....DC
- Protection..–0.5 to V_{cc} +0.5 V when configured as a digital signal, ±35 V when configured as an analog trigger signal or disabled, ±35 V powered off
- Accuracy...±1.0% of full scale range max

Digital Trigger

Compatibility ....TTL

Response ....Rising or falling edge

Pulse width ....10 ns min

RTSI

Trigger lines

- NI PCI/PXI-6052E 7
- NI DAQPad-6052E 4

Clock line...1

Bus Interface

Type

- NI PCI/PXI-6052E ....Master, Slave
- NI DAQPad-6052E for 1394...........Master, Slave, Asynchronous, 400 Mb/s

Power Requirement

Power available at I/O connector .... +4.65 VDC to +5.25 VDC at 1 A

NI PCI/PXI-6052E
+5 VDC (±5%) .... 1.3 A
(does not include current drawn from 5 V fuse on I/O connector)

NI DAQPad-6052E for 1394
9–24 VDC .... 20 W

Physical

Dimensions (not including connectors)
- NI PCI-6052E .... 17.5 by 10.6 cm (6.9 by 4.2 in.)
- NI PXI-6052E .... 16 by 10 cm (6.3 by 3.9 in.)
- NI DAQPad-6052E for 1394 .... 30.7 by 25.4 by 4.3 cm (12.1 by 10 by 1.7 in.)

I/O connector
- NI PCI/PXI-6052E .... 68-pin male SCSI-II type
- NI DAQPad-6052E .... 68-pin male SCSI-II type, or 15 BNCs and 30 removable screws

Environment

Operating temperature .... 0 to 55 °C

Storage temperature .... –20 to 70 °C

Relative humidity .... 5 to 90%, noncondensing

B

Custom Cabling and Optional Connectors

This appendix describes the cabling and connector options.

Custom Cabling

NI offers cables and accessories for use in prototyping your application or for use if you frequently change device interconnections.

If you want to develop your own cable, however, use the following guidelines:

- For the AI signals, use shielded twisted-pair wires for each AI pair, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from NI (part number 776832-01). The following list gives recommended part numbers for other connectors that mate to the I/O connector on the NI 6052E device:

- Honda 68-position, solder cup, female connector (part number PCS-E68FS)
- Honda backshell (part number PCS-E68LKPA)

Optional Connectors

Refer to Figure 4-1, *I/O Connector Pin Assignment for the NI 6052E,* for the pin assignments for the 68-pin connector. This connector is available when you use the SH6868EP or R6868 cable assemblies with the NI 6052E device.

Figure B-1 shows the pin assignments for the 50-pin connector. This connector is available when you use the SH6850 or R6850 cable assemblies.

AIGND	1	2	AIGND
ACH0	3	4	ACH8
ACH1	5	6	ACH9
ACH2	7	8	ACH10
ACH3	9	10	ACH11
ACH4	11	12	ACH12
ACH5	13	14	ACH13
ACH6	15	16	ACH14
ACH7	17	18	ACH15
AISENSE	19	20	DAC0OUT
DAC1OUT	21	22	EXTREF
AOGND	23	24	DGND
DIO0	25	26	DIO4
DIO1	27	28	DIO5
DIO2	29	30	DIO6
DIO3	31	32	DIO7
DGND	33	34	+5 V
+5 V	35	36	SCANCLK
EXTSTROBE*	37	38	PFI0/TRIG1
PFI1/TRIG2	39	40	PFI2/CONVERT*
PFI3/GPCTR1_SOURCE	41	42	PFI4/GPCTR1_GATE
GPCTR1_OUT	43	44	PFI5/UPDATE*
PFI6/WFTRIG	45	46	PFI7/STARTSCAN
PFI8/GPCTR0_SOURCE	47	48	PFI9/GPCTR0_GATE
GPCTR0_OUT	49	50	FREQ_OUT

Figure B-1. 50-Pin Connector Pin Assignments

C

Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of the device.

General Information

What is the DAQ-STC?

The DAQ-STC is the system timing control application-specific integrated circuit (ASIC) designed by NI and is the backbone of the E Series devices. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into the following three groups:

- AI—two 24-bit, two 16-bit counters
- AO—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be independently configured with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities such as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate are possible.

What does sampling rate mean to me?

Sampling rate is the fastest you can acquire data on the device and still achieve accurate results. For example, the PCI-6052E has a sampling rate of 333 kS/s. This sampling rate is aggregate: one channel at 333 kS/s or two channels at 166.5 kS/s per channel illustrates the relationship. Notice, however, that the PCI-6052E has settling times that vary with gain and accuracy. See Appendix A, *Specifications*, for exact specifications.

What type of +5 V protection do the PCI-6052E, PXI-6052E, and DAQPad-6052E have?

The PCI-6052E, PXI-6052E, and DAQPad-6052E for 1394 have +5 V lines equipped with a self-resetting 1 A fuse.

Installing and Configuring the Device

How do you set the base address for a PCI-6052E or PXI-6052E?

The base address of the PCI-6052E and PXI-6052E is automatically assigned through the PCI bus protocol. This assignment is completely transparent to you.

What jumpers should I be aware of when configuring the device?

The PCI-6052E, PXI-6052E, and DAQPad-6052E are jumperless and switchless.

Which NI document should I read first to get started using DAQ software?

The NI-DAQ or application software release notes documentation is always the best starting place.

What version of NI-DAQ must I have to program the device?

You must have NI-DAQ version 6.5 or later for the PCI-6052E. The PXI-6052E requires NI-DAQ version 6.6 or later. The PCI/PXI-6053E requires NI-DAQ version 6.9 or later. The DAQPad-6052E requires version 6.9.2 or later. You can download NI-DAQ from the NI Web site at `ni.com/download`.

What is Firewire?

Firewire and IEEE 1394 are the same thing. Firewire was the original name when the technology was developed by Apple. Later, Apple turned over the specification to the IEEE for standardization. Firewire is a registered trademark of Apple.

Can I use a 400 Mb/s 1394 device with a 100 Mb/s device?

Yes. The bus, however, slows to the slowest speed. The 400 Mb/s 1394 device will operate faster if the 100 Mb/s device is removed from the bus.

How many devices can I hook up to a 1394 bus?

Up to 64 devices, including the PC, may be attached to a single 1394 bus. NI-DAQ will support up to 64 DAQ devices attached to a 1394 bus.

Can I hook up the 1394 bus any way I want?

No. You cannot have cycles in the bus cabling, and you must have fewer than 16 hops between devices.

What can I do to optimize the performance of the 1394 device?

There are several things that can be done to optimize the performance of the 1394 device. First, try to keep the bus running at the fastest speed possible by attaching only devices that are at least as fast as the 1394 device. If a 200 Mb/s device is added to the bus with the 400 Mb/s DAQ device, you will slow the entire bus down to 200 Mb/s. Second, minimize the maximum number of hops between the devices on the bus. The more hops you have, the slower the bus will run. Finally, remember there is only a limited amount of bandwidth available on the bus. If you stream digital video (DV) at 20 Mb/s, you will hurt the device performance.

Will 1394 DAQ work with Windows 95?

No. Microsoft and NI do *not* support Windows 95 with 1394. However, Microsoft and NI do support Windows 2000/Me/98se with 1394.

Analog Input and Output

I'm using my device in differential analog input mode, and I have connected a differential input signal, but my readings are random and drift rapidly. What's wrong?

Check the ground reference connections. The signal can be referenced to a level that is considered *floating* with reference to the device ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the device reference. There are various methods of achieving this while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Connecting the Signals*.

I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When a DAC switches from one voltage to another, it produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of the output signal. Refer to Chapter 3, *Hardware Overview*, the *Analog Output Reglitch* section, for more information about reglitching.

Can I synchronize a one-channel AI data acquisition with a one-channel AO waveform generation on the device?

Yes. Use the waveform-generation timing pulses to control the AI data acquisition. To do this, follow steps 1 through 4 below, in addition to the usual steps for data-acquisition and waveform-generation configuration.

1. Enable the PFI5 line for output, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW)`.
   - If you are using LabVIEW, invoke Route Signal VI with signal name set to PFI5 and signal source set to AO Update.
2. Set up data acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_CONVERT, ND_PFI_5, ND_HIGH_TO_LOW)`.
   - If you are using LabVIEW, invoke AI Clock Config VI with clock source code set to PFI pin, high to low, and clock source string set to 5.
3. Initiate analog input data acquisition, which will start only when the AO waveform generation starts.
4. Initiate AO waveform generation.

Timing and Digital I/O

What types of triggering can be hardware-implemented on my device?

Digital triggering and analog triggering are both hardware-supported.

What added functionality does the DAQ-STC make possible in contrast to the Am9513?

The DAQ-STC incorporates much more than just 10 Am9513-style counters within one chip. In fact, the DAQ-STC has the complexity of more than 24 chips. The DAQ-STC makes possible PFI lines, analog triggering, selectable logic level, and frequency shift keying. The DAQ-STC also makes buffered operations possible, such as direct up/down control, single or pulse train generation, equivalent time sampling, buffered period, and buffered semiperiod measurement.

What is the difference in timebases between the Am9513 counter/timer and the DAQ-STC?

The DAQ-STC-based MIO devices have a 20 MHz timebase.
The Am9513-based MIO devices have a 1 MHz or 5 MHz timebase.

Do the counter/timer applications that I previously wrote work with the DAQ-STC?

If you are using NI-DAQ with LabVIEW, some of your applications drawn using the CTR VIs do still run. However, there are many differences in the counters between the E Series and other devices. The counter numbers are different, timebase selections are different, and the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on devices without the DAQ-STC).

If you are using NI-DAQ or LabWindows/CVI, the counter/timer applications that you wrote previously do not work with the DAQ-STC. You must use the GPCTR functions. ICTR and CTR functions do not work with the DAQ-STC. The GPCTR functions have the same capabilities as the ICTR and CTR functions, plus more, but you must rewrite the application with the GPCTR function calls.

I'm using one of the general-purpose counter/timers on my E Series device, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?

If you are using NI-DAQ or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line.
By default, all timing I/O lines except EXTSTROBE* are tri-stated.

What are the PFIs and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you are using NI-DAQ or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, and Counter Set

Attribute advanced level VIs to indicate which function the connected signal will serve. Use the Route Signal VI to enable the PFI lines to output internal signals.

Table C-1. Signal Name Equivalencies

Hardware Signal Name	LabVIEW Route Signal	NI-DAQ Select_Signal
TRIG1	AI Start Trigger	ND_IN_START_TRIGGER
TRIG2	AI Stop Trigger	ND_IN_STOP_TRIGGER
STARTSCAN	AI Scan Start	ND_IN_SCAN_START
SISOURCE	—	ND_IN_SCAN_CLOCK_TIMEBASE
CONVERT*	AI Convert	ND_IN_CONVERT
AIGATE	—	ND_IN_EXTERNAL_GATE
WFTRIG	AO Start Trigger	ND_OUT_START_TRIGGER
UPDATE*	AO Update	ND_OUT_UPDATE
UISOURCE	—	ND_OUT_UPDATE_CLOCK_TIMEBASE
AOGATE	—	ND_OUT_EXTERNAL_GATE

Caution If you enable a PFI line for output, do *not* connect any external signal source to it. If you do, you can damage the device, the computer, and the connected equipment.

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high impedance by the hardware. This means that the device circuitry is not actively driving the output either high or low. However, these lines can have pull up or pull down resistors connected to them as shown in Table 4-1, *I/O Connector Signal Descriptions*, and Table 4-2, *I/O Signal Summary*. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) is in the high impedance state after power on, and Table 4-1, *Pins Used by the NI PXI-6052E*, shows that there is a 50 kΩ pull-up resistor. This pull-up resistor sets the DIO(0) pin to a logic high when the output is in a high-impedance state.

D

Technical Support Resources

Web Support

National Instruments Web support is your first stop for help in solving installation, configuration, and application problems and questions. Online problem-solving and diagnostic resources include frequently asked questions, knowledge bases, product-specific troubleshooting wizards, manuals, drivers, software updates, and more. Web support is available through the Technical Support section of `ni.com`.

NI Developer Zone

The NI Developer Zone at `ni.com/zone` is the essential resource for building measurement and automation systems. At the NI Developer Zone, you can easily access the latest example programs, system configurators, tutorials, technical news, as well as a community of developers ready to share their own techniques.

Customer Education

National Instruments provides a number of alternatives to satisfy your training needs, from self-paced tutorials, videos, and interactive CDs to instructor-led hands-on courses at locations around the world. Visit the Customer Education section of `ni.com` for online course schedules, syllabi, training centers, and class registration.

System Integration

If you have time constraints, limited in-house technical resources, or other dilemmas, you may prefer to employ consulting or system integration services. You can rely on the expertise available through our worldwide network of Alliance Program members. To find out more about our Alliance system integration solutions, visit the System Integration section of `ni.com`.

Worldwide Support

National Instruments has offices located around the world to help address your support needs. You can access our branch office Web sites from the Worldwide Offices section of ni.com. Branch office Web sites provide up-to-date contact information, support phone numbers, e-mail addresses, and current events.

If you have searched the technical support resources on our Web site and still cannot find the answers you need, contact your local office or National Instruments corporate. Phone numbers for our worldwide offices are listed at the front of this manual.

Glossary

Prefix	Meanings	Value
n-	nano-	10^{-9}
μ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Numbers/Symbols

%	percent
+	positive of, or plus
–	negative of, or minus
>	greater than
≥	greater than or equal to
<	less than
≤	less than or equal to
/	per
°	degree
Ω	ohm
$\sqrt{}$	square root of
+5 V	+5 VDC source signal

A

A	amperes
A/D	analog-to-digital
AC	alternating current
ACH	analog input channel signal
ActiveX controls	a special form of Automation Object. ActiveX Controls are similar to Visual Basic custom controls (VBXs), but their architecture is based on OLE; ActiveX Controls can be freely plugged into any OLE-enabled development tool, application, or Web browser
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
ADE	application development environment—an application designed to make it easier for a user to develop software
AI	analog input
AIGATE	analog input gate signal
AIGND	analog ground signal
AISENSE	analog sense signal
ANSI	American National Standards Institute
AO	analog output
AOGND	analog output ground signal
ASIC	Application-Specific Integrated Circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions for a specific customer

B

bipolar	a signal range that includes both positive and negative values (for example, –5 V to +5 V)
BNC	coaxial connector
buffer	temporary storage for acquired or generated data (software)
bus	the group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. An examples of a PC bus is the PCI bus.

C

C	Celsius
CalDAC	calibration DAC
CH	channel—pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.
clock	hardware component that controls timing for reading from or writing to groups
cm	centimeter
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio—a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB)
common-mode noise	unwanted signals that appear in equal phase and amplitude on both the inverting and noninverting input in a differential measurement system. Ideally, but not completely in practice, the measurement device ignores this noise, because the measurement device is designed to respond to the difference between the inverting and noninverting inputs.
CONVERT*	convert signal

counter/timer	a circuit that counts external pulses or clock pulses (timing)
CTR	counter

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal
DAQ	data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer
DAQ-STC	data acquisition system timing controller chip
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: $dB=20\log_{10} (V_1/V_2)$, for signals in volts
DC	direct current
DGND	digital ground signal
DIFF	differential mode
differential input	an analog input consisting of two terminals, both of which are isolated from computer ground, whose difference is measured
DIO	digital input/output
DIP	dual inline package
dithering	the addition of Gaussian noise to an analog input signal

DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	differential nonlinearity—a measure in least significant bit of the worst-case deviation of code widths from their ideal value of 1 LSB
DO	digital output

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
EXTREF	external reference signal
EXTSTROBE	external strobe signal

F

F	farads
FIFO	first-in first-out memory buffer—the first data stored is the first data sent to the acceptor. FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be retrieved or output. For example, an analog input FIFO stores the results of A/D conversions until the data can be retrieved into system memory, a process that requires the servicing of interrupts and often the programming of the DMA controller. This process can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored on the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.
floating signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called nonreferenced signal sources. Some common example of floating signal sources are batteries, transformers, or thermocouples.
FREQ_OUT	frequency output signal

FS	floating source
ft	feet

G

GPCTR0_GATE	general purpose counter 0 gate signal
GPCTR0_OUT	general purpose counter 0 output signal
GPCTR0_SOURCE	general purpose counter 0 clock source signal
GPCTR0_UP_DOWN	general purpose counter 0 up down
GPCTR1_GATE	general purpose counter 1 gate signal
GPCTR1_OUT	general purpose counter 1 output signal
GPCTR1_SOURCE	general purpose counter 1 clock source signal
GPCTR1_UP_DOWN	general purpose counter 1 up down
GS	grounded source

H

Hz	hertz—the number of scans read or updates written per second
hysteresis	lag between making a change and the effect of the change

I

I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
I_{OH}	current, output high
I_{OL}	current, output low
INL	integral nonlinearity—a measure in LSB of the worst-case deviation from the ideal A/D or D/A transfer characteristic of the analog I/O circuitry

L

LED	light emitting diode—used to indicate device status
LSB	least significant bit

M

m	meters
MB	megabytes of memory
MIO	multifunction I/O
MITE	MXI Interface to Everything—a custom ASIC designed by National Instruments that implements the PCI bus interface. The MITE supports bus mastering for high-speed data transfers over the PCI bus.
MSB	most significant bit
mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel

N

NC	normally closed, or not connected
NI	National Instruments
NI-DAQ	National Instruments driver software for DAQ hardware
noise	an undesirable electrical signal—noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, soldering irons, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
nonreferenced signal sources	signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called floating signal sources. Some common example of nonreferenced signal sources are batteries, transformers, or thermocouples.

NRSE	nonreferenced single-ended mode—all measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground

O

OUT	output pin—a counter output pin where the counter can generate various TTL pulse waveforms

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
PFI	programmable function input
PFI0/TRIG1	PFI0/trigger 1
PFI1/TRIG2	PFI1/trigger 2
PFI2/CONVERT*	PFI2/convert
PFI3/GPCTR1_ SOURCE	PFI3/general purpose counter 1 source
PFI4/GPCTR1_ GATE	PFI4/general purpose counter 1 gate
PFI5/UPDATE*	PFI5/update
PFI6/WFTRIG	PFI6/waveform trigger
PFI7/STARTSCAN	PFI7/start of scan
PFI8/GPCTR0_ SOURCE	PFI8/general purpose counter 0 source
PFI9/GPCTR0_ GATE	PFI9/general purpose counter 0 gate

PGIA	programmable gain instrumentation amplifier
port	(1) a communications connection on a computer or a remote controller (2) a digital port, consisting of four or eight lines of digital input and/or output
ppm	parts per million
pu	pullup
PXI	PCI eXtenstions for Instrumentation—a rugged, open system for modular instrumentation based on CompactPCI, with special mechanical, electrical, and software features. The PXIbus standard was originally developed by National Instruments in 1997, and it is now managed by the PXIbus Systems Alliance.

R

referenced signal sources	signal sources with voltage signals that are referenced to a system ground, such as the earth or a building ground. Also called grounded signal sources.
reglitch	circuitry used on analog outputs to generate uniform glitch energy at every code rather than large glitches at the major code transitions. This uniform glitch energy appears as a multiple of the update rate in the frequency spectrum.
rms	root mean square—the square root of the average value of the square of the instantaneous signal amplitude; a measure of signal amplitude
RSE	referenced single-ended mode—all measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system.
RTD	resistance temperature detector—a metallic probe that measures temperature based upon its coefficient of resistivity
RTSI bus	real-time system integration bus—the National Instruments timing bus that connects DAQ devices directly, by means of connectors on top of the devices, for precise synchronization of functions

S

s	seconds
S	samples
S/s	samples per second—used to express the rate at which a DAQ device samples an analog signal
SCANCLK	scan clock signal
SCXI	Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ devices in the noisy PC environment
settling time	the amount of time required for a voltage to reach its final value within specified limits
signal conditioning	the manipulation of signals to prepare them for digitizing
SISOURCE	SI counter clock signal
source impedance	a parameter of signal sources that reflects current-driving ability of voltage sources (lower is better) and the voltage-driving ability of current sources (higher is better)
STARTSCAN	start scan signal
system noise	a measure of the amount of noise seen by an analog circuit or an ADC when the analog inputs are grounded

T

TC	terminal count—the highest value of a counter
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gw}	gate pulse width
THD	total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage

thermocouple	a temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.
TIO	timing input/output
TRIG	trigger signal
trigger	any event that causes or starts some form of data capture
t_{out}	output delay time
t_{sc}	source clock period
t_{sp}	source pulse width
TTL	transistor-transistor logic
two's complement	given a number *x* expressed in base 2 with *n* digits to the left of the radix point, the (base 2) number 2*n* - *x*

U

UI	update interval
UISOURCE	update interval counter clock signal
unipolar	a signal range that is always positive (for example, 0 to +10 V)
update	the output equivalent of a scan. One or more analog or digital output samples. Typically, the number of output samples in an update is equal to the number of channels in the output group. For example, one pulse from the update clock produces one update which sends one new sample to every analog output channel in the group.
UPDATE	update signal

V

V	volts
Vcc	positive voltage supply
VDC	volts direct current

VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument; (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	volts in
V_m	measured voltage
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{out}	volts out
V_{ref}	reference voltage
Vrms	volts, root mean square

W

W	watts
waveform	multiple voltage readings taken at a specific sampling rate
WFTRIG	waveform generation trigger signal

Index

Symbols

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